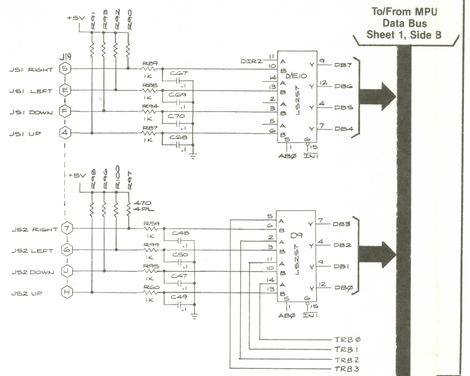
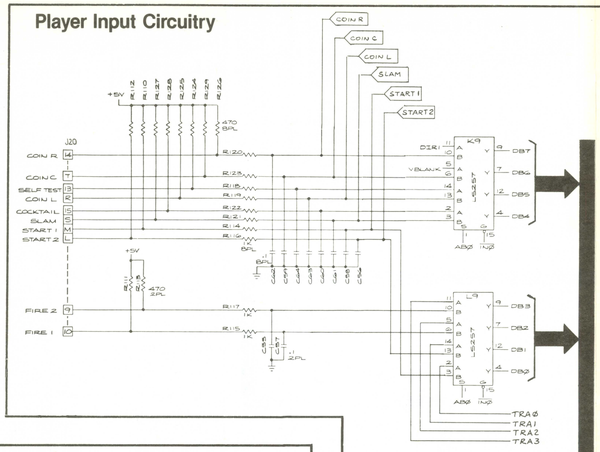
Joystick Circuitry



Player Input Circuitry



Testing the Player Inputs

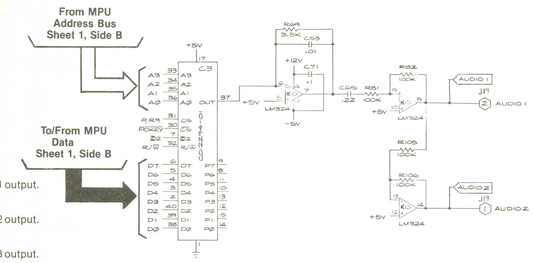
1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0C00 (self-test switch only) or 0C01 (all others).
   e. R/W MODE to STATIC
3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2
4. The DATA DISPLAY will change if the switches are operating properly.

Testing the Audio Outputs

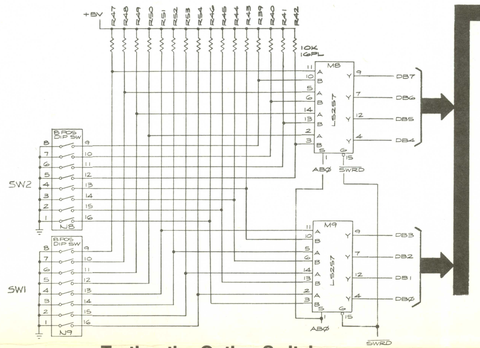
1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to WRITE
   d. Key in address or press ADDRESS INCR
   e. Press DATA SET
   f. Key in data
   g. Set R/W MODE to PULSE, then to OFF.
   h. For each address, repeat sequence starting at Step d.

ADDRESS	DATA	RESULTS
100F	00	
100F	03	
1000	55	
1001	AF	Pure tone is heard from channel 1 output.
1001	00	Channel 1 output is turned off.
1002	55	
1003	AF	Pure tone is heard from channel 2 output.
1003	00	Channel 2 output is turned off.
1004	55	
1005	AF	Pure tone is heard from channel 3 output.
1005	00	Channel 3 output is turned off.
1006	55	
1007	AF	Pure tone is heard from channel 4 output.
1007	00	Channel 4 output is turned off.

Audio Output Circuitry



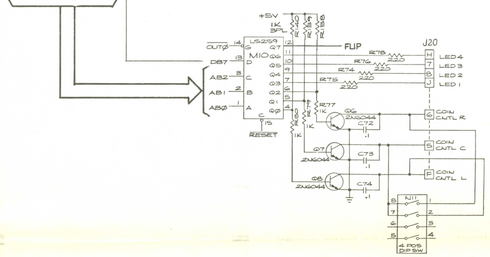
Option Input Circuitry



Testing the Option Switches

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0800 (N9) or 0801 (N8)
   e. R/W MODE to STATIC
3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

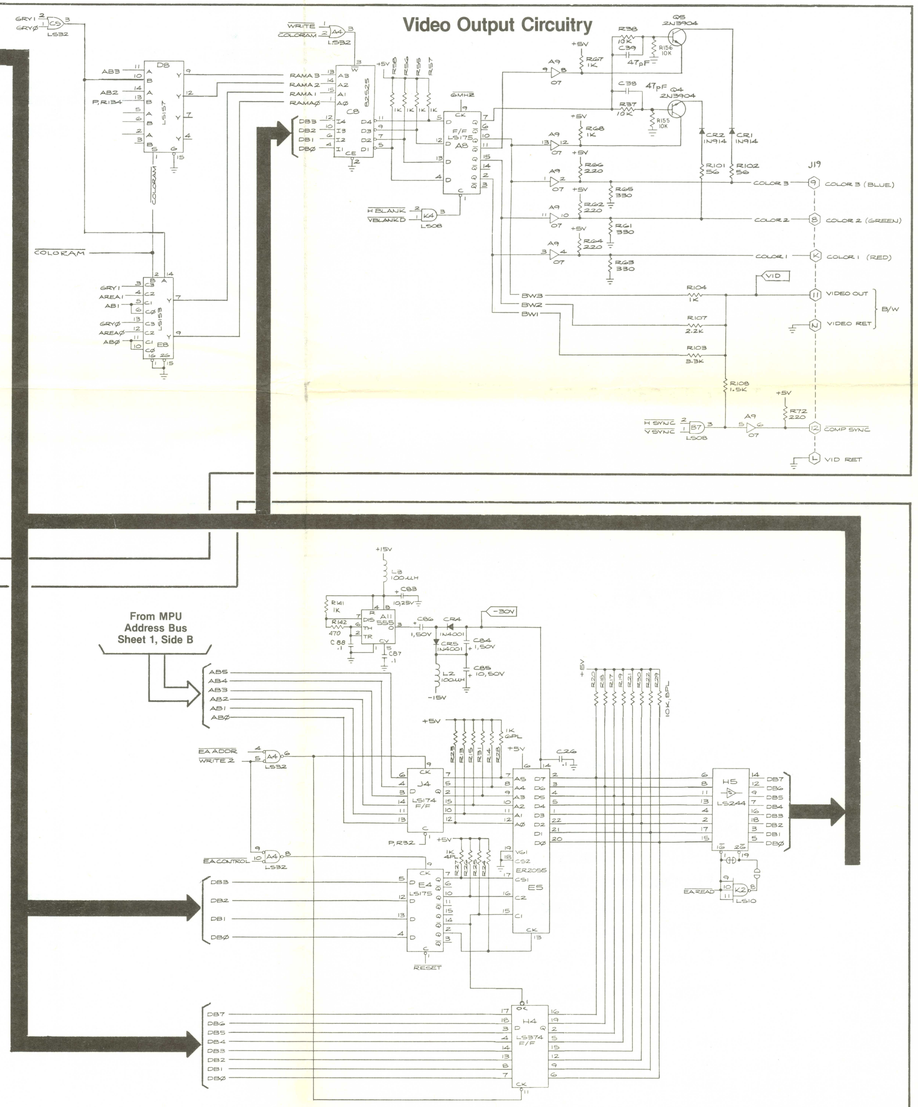
Coin Counter Output Circuitry



Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on AB0-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Video Output Circuitry



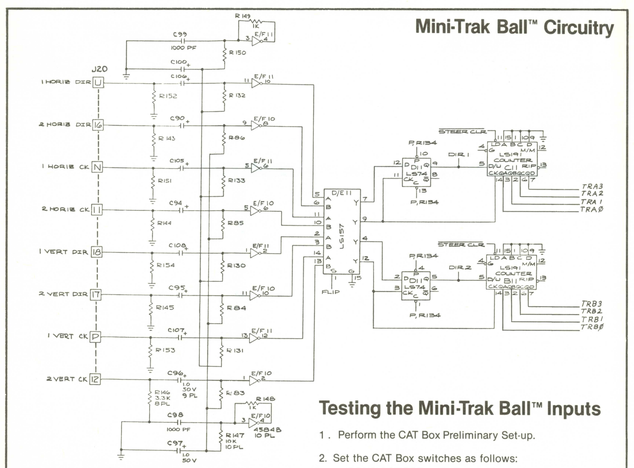
The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by E8. The output, selected by GRY0 or GRY1, is RAMA0-RAMA3 (RAM ADDRESS).

RAMA0-RAMA3 are applied to color RAM C8. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (C8 pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green) and COLOR 3 (blue), provide 6 extra colors for a total of 14.

1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 3. The result is a pale blue when COLOR 1 and COLOR 2 are off.
2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 2. The result is a pale green when COLOR 1 and COLOR 3 are off.

Mini-Trak Ball™ Circuitry



Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0C00 (vertical) or 0C02 (horizontal)
   e. R/W MODE to PULSE
3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.

High Score Memory Circuitry

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5 and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to −29V. When the signal is 0V, CR5 is cutoff and CR4 is forward-biased which causes C84 to develop a charge. C84 charges to approximately −28V. This is the potential required for EAROM C0 to operate.

The MPU addresses the EAROM (AB0-AB5) when a low EAADDR gates WRITE2 at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low EACONTROL gates WRITE2 at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when EAREAD on pin 1 of buffer H4 goes low.

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