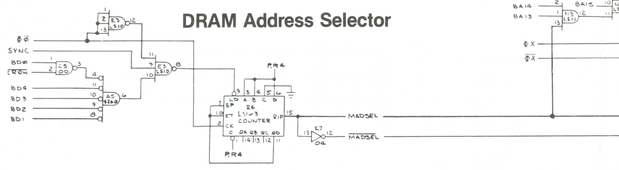
IRQH *(Hardware Interrupt)* - Signal that disables the DRAM Address Controller from putting out a high MADSEL signal.

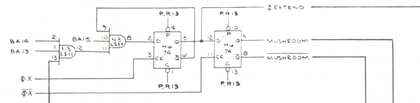
DRAM Address Selector



SYNC - Signal generated directly from the microprocessor that occurs at the beginning of an instruction read cycle and lasts one cycle of microprocessor Φ2 clock. Five Φ0 cycles later, MADSEL goes high.

MADSEL *(Multiplexed Address Select)* - Microprocessor-generated signal that, when high, enables the microprocessor to write or read 2- or 3-color bit data into or out of the DRAM. MADSEL and MUSHROOM together select the address inputs, the data inputs and the actual DRAM chips to be written to or read from. MADSEL also, along with high MUSHROOM and ΦX enables the latching of 2-color bit data in the Microprocessor Data Input Interface circuit. See tables in DRAM Write Enable and DRAM Data input Selector circuits.

3rd Color Bit Select

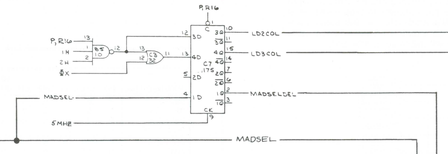


ΦEXTEND *(Clock Extend)* - Microprocessor-generated signal that, when high, delays the Φ0 clock input (holds Φ0 high) to the microprocessor while the microprocessor accesses the 3rd-color bit region of the DRAM.

ΦX *(Phase X)* - Sync-generated signal equivalent to 2H (1.25 MHz), except during the last 32 scan lines (cities area) of the video display. At this time ΦX pulses high on every other high pulse of 2H (0.625 MHz).

Φ0 *(Microprocessor Clock Input)* - Sync-generated signal, controlled by the microprocessor and sync that is the basic clock input to the microprocessor.

DRAM Picture Output Enable

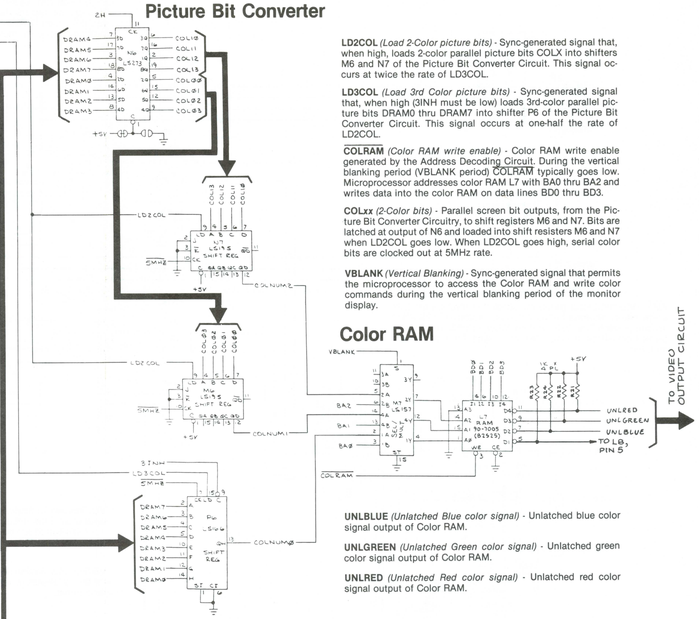


MADSEL

MUSHROOM

MUSHROOM	MADSEL	MD0	MD1	MD2	MD3	MD4	MD5	MD6	MD7
LOW	LOW	D7	D6	D5	D4	D3	D2	D1	D0
HIGH	LOW	Invalid State							
LOW	HIGH	D7	D7	D7	D6	D6	D6	D6	D6
HIGH	HIGH	D5	D5	D5	D5	D5	D5	D5	D5

Picture Bit Converter



LD2COL *(Load 2-Color picture bits)* - Sync-generated signal that, when high, loads 2-color parallel picture bits COLX into shifters M6 and N7 of the Picture Bit Converter Circuit. This signal occurs at twice the rate of LD3COL.

LD3COL *(Load 3rd Color picture bits)* - Sync-generated signal that, when high (3INH must be low) loads 3rd-color parallel picture bits DRAM0 thru DRAM7 into shifter P6 of the Picture Bit Converter Circuit. This signal occurs at one-half the rate of LD2COL.

COLRAM *(Color RAM write enable)* - Color RAM write enable generated by the Address Decoding Circuit. During the vertical blanking period (VBLANK period) COLRAM typically goes low. Microprocessor addresses color RAM L7 with BA0 thru BA2 and writes data into the color RAM on data lines BD0 thru BD3.

COLxx *(2-Color bits)* - Parallel screen bit outputs, from the Picture Bit Converter Circuitry, to shift registers M6 and N7. Bits are latched at output of M6 and loaded into shift resisters M6 and N7 when LD2COL goes low. When LD2COL goes high, serial color bits are clocked out at 5MHz rate.

VBLANK *(Vertical Blanking)* - Sync-generated signal that permits the microprocessor to access the Color RAM and write color commands during the vertical blanking period of the monitor display.

Color RAM

UNLBLUE *(Unlatched Blue color signal)* - Unlatched blue color signal output of Color RAM.

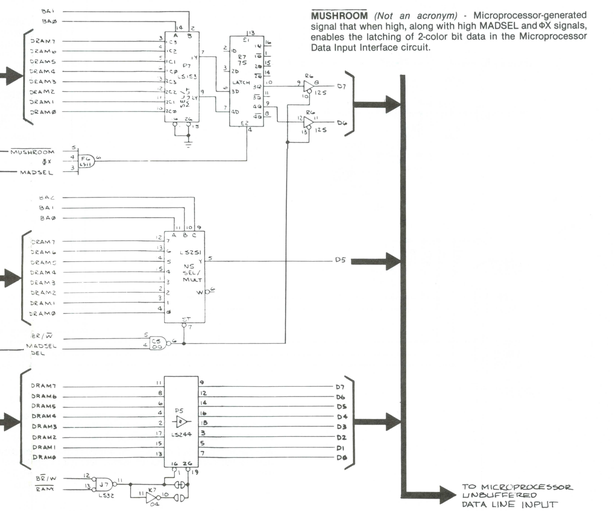
UNLGREEN *(Unlatched Green color signal)* - Unlatched green color signal output of Color RAM.

UNLRED *(Unlatched Red color signal)* - Unlatched red color signal output of Color RAM.

3INH *(Third-color bit Inhibit)* - Sync-generated signal that, when high, prohibits a 3rd-color bit output from the Picture Bit Converter circuit. 3INH goes low during the last 32 scan lines (cities area) of the video display.

MADSEL — TO SHEET 1, SIDE B ADDRESS DECODING CIRCUIT

Microprocessor Data Input Interface



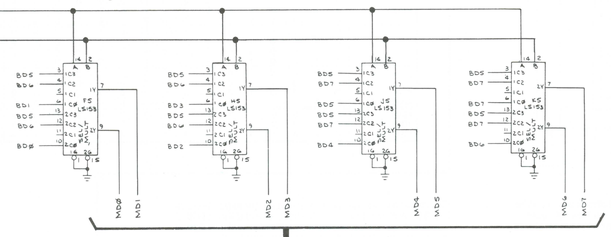
MUSHROOM *(Not an acronym)* - Microprocessor-generated signal that when high, along with high MADSEL and ΦX signals, enables the latching of 2-color bit data in the Microprocessor Data Input Interface circuit.

MADSELDEL *(Multiplexed Address Select Delayed)* -Microprocessor-generated signal delayed one pulse of 5MHz from MADSEL signal. When MADSELDEL is high, along with high BR/W, microprocessor reads DRAM data output through Microprocessor Data Input Interface. MADSELDEL also disables Microprocessor Address Decoding Circuit.

BR/W *(Buffered Read/Write)* - Microprocessor-generated signal that, when high, enables the microprocessor to write or read the 3rd-color bit data into the DRAM. MUSHROOM and MADSEL together select the address inputs, the data inputs and the actual DRAM chips to be written to or be read from. See tables in DRAM Write Enable and DRAM Data Input Selector circuits.

CAS *(Column Address Strobe)* - Sync-generated strobe that, along with RAS and DEADSEL, sets up the address input to the DRAM. RAS sets up the seven row-address bits and latches the bit inputs for the DRAM row address. CAS sets up the seven column-address bits and latches the bit inputs for the DRAM column address. DEADSEL selects the origin of the seven address-bit inputs.

DRAM Data Input Selector

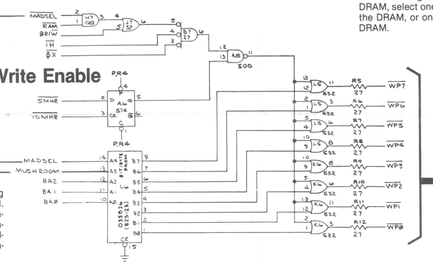


Address Input	WP0	WP1	WP2	WP3	WP4	WP5	WP6	WP7	
0-15	0	0	0	0	0	0	0	0	
16	0	1	1	1	0	1	1	1	
17	1	0	1	1	0	1	1	1	
18	1	1	0	1	1	1	0	1	
19	1	1	1	0	1	1	1	0	2-color bit data
20	0	1	1	1	0	1	1	1	
21	1	0	1	1	1	0	1	1	
22	1	1	0	1	1	1	0	1	
23	1	1	1	0	1	1	1	0	
24	0	1	1	1	0	1	1	1	
25	1	0	1	1	1	0	1	1	
26	1	1	0	1	1	1	0	1	
27	1	1	1	0	1	1	1	0	3rd-color bit data
28	1	1	1	1	0	1	1	1	
29	1	1	1	1	1	0	1	1	
30	1	1	1	1	1	1	0	1	
31	1	1	1	1	1	1	1	0	

WPx *(Write enable Pulses)* - Microprocessor-generated signals that select eight DRAM chips in the working RAM area of the DRAM, select one pair of DRAM chips in the 2-color bit region of the DRAM, or one DRAM chip in the 3rd-color bit region of the DRAM.

MDx *(Multiplexed Data)* - Data line to the DRAM from the microprocessor, selected by MADSEL and MUSHROOM signal. Table DRAM Data Input Selector Circuit defines source, controlled by MADSEL and MUSHROOM signals.

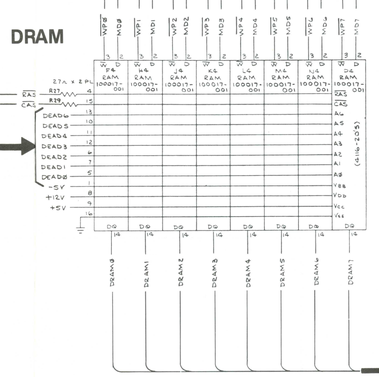
DRAM Write Enable



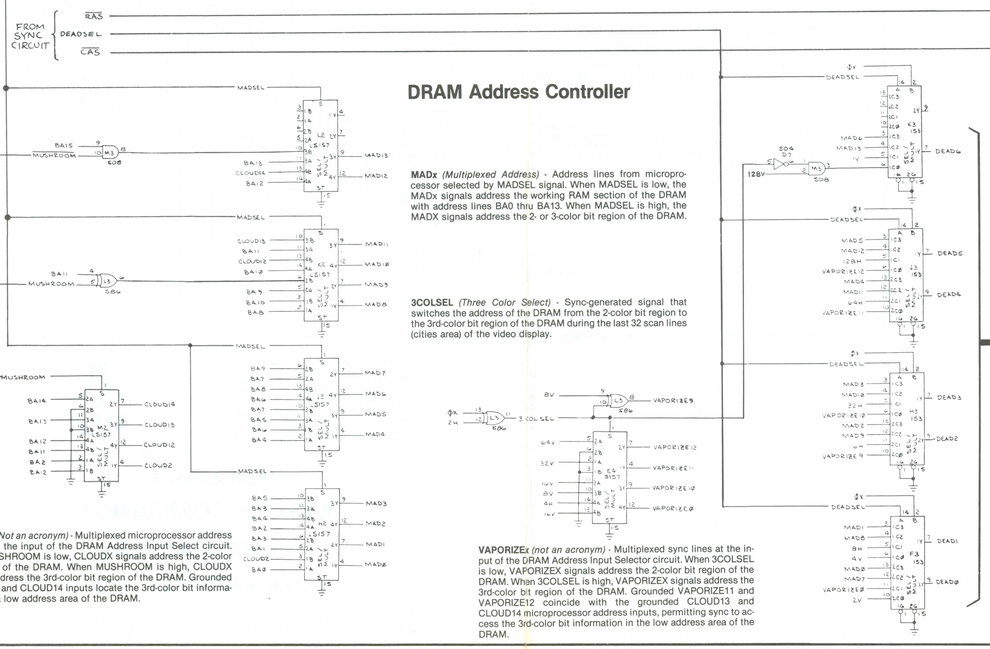
DEADSEL *(Address Select)* - Sync-generated strobe that, along with RAS and CAS, sets up the address input of the DRAM. RAS strobes the DRAM to latch the row-address inputs. CAS strobes the DRAM to latch the column-address inputs. When high, DEADSEL selects the row-address inputs. When low, DEADSEL selects the column-address inputs.

RAS *(Row Address Strobe)* - Sync-generated strobe that, along with CAS and DEADSEL, sets up the address input to the DRAM. RAS sets up the seven new address bits and latches the bit inputs for the DRAM row address. CAS sets up the seven column-address bits and latches the bit inputs for the DRAM column address. DEADSEL selects the origin of the seven address bit inputs.

DRAM



DRAM Address Controller



MADx *(Multiplexed Address)* - Address lines from microprocessor selected by MADSEL signal. When MADSEL is low, the MADx signals address the working RAM section of the DRAM with address lines BA0 thru BA13. When MADSEL is high, the MADX signals address the 2- or 3-color bit region of the DRAM.

3COLSEL *(Three Color Select)* - Sync-generated signal that switches the address of the DRAM from the 2-color bit region to the 3rd-color bit region of the DRAM during the last 32 scan lines (cities area) of the video display.

CLOUDx *(Not an acronym)* - Multiplexed microprocessor address lines from the input of the DRAM Address Input Select circuit. When MUSHROOM is low, CLOUDX signals address the 2-color bit region of the DRAM. When MUSHROOM is high, CLOUDX signals address the 3rd-color bit region of the DRAM. Grounded CLOUD13 and CLOUD14 input locations locate the 3rd-color bit information into a low address area of the DRAM.

VAPORIZEx *(not an acronym)* - Multiplexed sync lines at the input of the DRAM Address Input Selector circuit. When 3COLSEL is low, VAPORIZEX signals address the 2-color bit region of the DRAM. When 3COLSEL is high, VAPORIZEX signals address the 3rd-color bit region of the DRAM. Grounded VAPORIZE11 and VAPORIZE12 coincide with the grounded CLOUD13 and CLOUD14 microprocessor address inputs, permitting sync to access the 3rd-color bit information in the low address area of the DRAM.

DEADx *(DRAM Address)* - Column- and row-address inputs to the DRAM selected by DEADSEL and ΦX. When DEADSEL is high, DEADX signals are row-address inputs to DRAM. When DEADSEL is low, DEADX signals are column-address inputs to DRAM. When ΦX is low, DEADX address inputs are from Sync Circuit. When ΦX is high, DEADX address inputs are from microprocessor address lines.

DRAMx *(DRAM data output bits)* - Data output bits from the DRAM. The DRAMx signals are converted to serial data by the Picture Bit converter Circuit, then address the Color RAM. The microprocessor reads working RAM data DRAM0 thru DRAM7 through P5 in the Microprocessor Data Input Interface when RAM and BR/W are low. The microprocessor reads selected picture data bits when BR/W and MADSELDEL are high on data lines D5, D6 and D7.

Sheet 2, Side A

MISSILE COMMAND™

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