Bally Midway's

MCR II-III Systems

General Information and Troubleshooting Procedures Micro-Processor Video Games

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Introduction

This manual has been written for video games which utilize Bally Midway's MCR II System. It offers generalized troubleshooting procedures for common types of malfunctions which can be applied to most video games. We will not attempt to give you specific instructions for troubleshooting particular games because this would involve hundreds of pages of more or less repetitive instructions, differing only in the specific details of each game.

The most common problems occur in harness components such as the coin acceptor, player controls, interconnecting wiring, etc. These areas are covered in moderate detail.

The TV Monitor and Game Logic Printed Circuit Boards (PCB's) provide their fair share of problems too, but not to the extent of the harness and its component parts.

As you already know, the Game Logic PC Boards are complex devices. Each contains a great number of different interrelated circuits. However, Bally Midway's MCR II System has been designed in such a manner as to allow it to use the **SAME** PCB's for **MANY** different games. The major changes which give each game its own particular individuality are accomplished in the EPROMS and other Integrated Circuit devices that are installed on each of these PC Boards.

With regard to the TV Monitors, we are including the same information at the end of this manual which goes into each OPERATOR'S MANUAL we send out. Covered will be Color Monitors **AND** Black and White X-Y Monitors in 13" and 19" sizes by Wells Gardner and Electrohome.

General Troubleshooting Suggestions

The first step in troubleshooting is to correctly identify the malfunctions symptoms. This includes not only the circuits or features malfunctioning, but also those still operational. A carefully trained eye will pick up other clues to what's wrong as well. For instance, a game in which the computer functions fail completely just after money was collected may have a quarter shorting the PCB traces. Often an experienced troubleshooter will be able to spot the cause of a problem even before opening the cabinet.

After all the clues are carefully considered, the possible malfunctioning areas can be narrowed down to one or two good suspects. Those areas can be examined by a process of elimination until the cause of the malfunction is discovered.

Harness Component Troubleshooting

Typical problems falling in this category are coin and credit problems, power problems, and failure of individual features.

NO GAME CREDIT — For example, a prospective game player inserts a quarter or token and is not awarded a game. The first thing to check is whether or not the quarter or token is returned. If it was returned, the malfunction most certainly lies in the coin acceptor itself. First, use a set of test coins (both old and new) to ascertain that the player's coin is not undersize or underweight. If your test coins are also returned, coin acceptor servicing is indicated. Generally, the cause of this particular problem is a maladjusted magnet gate. Normally, this will mean slightly closing the magnet gate by turning the adjusting screw out a bit.

If the quarter or token is not returned and there is no game credit, the cause of the malfunction may be in one of several areas. First, try operating the coin return button; if the coin is returned, the problem is most likely in the magnet gate. Enlarge the gap according to the coin acceptor manufacturer's service procedures. If this does not cure the problem, remove the coin acceptor, clean it, and perform the manufacturer's suggested major adjustment procedure.

If the trapped coin is not returned when the wiper lever is actuated, you may have an acceptor jammed by a slug, gummed up with beer, a jammed coin chute, or mechanical failure of the acceptor mechanism. In this case, first check for the slug that will generally be trapped against the magnet. If a slug is found, simply remove it and test the acceptor. If the chute is blocked, remove the acceptor and remove the jammed coins. If there is actual failure of the acceptor, remove the unit and repair as indicated by the acceptor manufacturer's service procedures.

If the coin is making its way through the acceptor (that is, falling into the coin box), yet there is still no game credit, you either have a mechanical failure of the coin switch or electrical failure of the coin and credit circuits. The first place to begin is by checking the coin switch. Most of these switches are the make/break variety of micro switch. They are checked for continuity between the "NO", "NC", and "C" terminals. When **not** actuated, the "NC" and "C" terminals should be continuous and the "NO" terminal open. When actuated, the "NO" and "C" terminals should be continuous and the "NC" terminal open. If the coin switch checks good, inspect the solder connections to the coin switch terminals to be sure there is good contact at this point. If necessary, use a continuity tester and check from the terminal lug on the switch to the associated PCB trace. This will tell you if there is a continuous line all the way to the credit circuit.

If the coin switch wires do check good, the problem is in one of the game logic boards — most likely in the coin and credit circuitry.

If you do get a game credit when a coin is desposited, but the game will not start when the one or two player start button is pressed, there may be a problem in the start switch, the interconnecting wiring, or the game logic boards. First, check the switch. If the switch is OK, proceed to check the wiring. Again, make sure you go from the terminal lug on the switch to the PCB trace. This way, you will check the terminal contact as well as the PCB edge connector contact. If the wiring is continuous, proceed to check the PCB credit circuit. If not, check each section of the wiring, until the discontinuity is located. If the wiring is OK, the problem must lie in the game's logic boards.

Transformer and Line Voltage Problems

Your game **MUST** have the correct line voltage to operate properly. If the line voltage drops too low, one of the game's logic circuits will disable the credit acceptance circuit. The point at which the game's logic circuits will fail to function is approximately 105 volts AC.

Low line voltage may have many causes. Line voltage normally fluctuates a certain amount during the day as the total usage varies. Peak usage times occur mainly at dawn and/or dusk. So if your game's problem seems to be related to the time of day, this may be a factor. A large load connected to the same line as the game (such as a large air conditioner or other device with an exceptionally large electric motor) may drop the line voltage significantly when starting up. This drop can result in an intermittent credit problem. In addition, poor connections in the location wiring, plug, or line cord may also cause a significant drop in power. Cold solder joints in the game's harness, especially in areas like the transformer connections, interlock switch, or fuse block, may also produce the same results, although probably on a more permanent basis.

Sometimes location owners (especially in bars) replace light switches with dimmer rheostats, and the game is sometimes on the same line. Obviously, the voltage available to the game is going to drop dramatically when the dimmer is turned down.

In any case, the way to check for proper line voltage is with your VOM. Set the VOM to the 250 VAC scale and stick the probes into the wall outlet the game was connected to. If it's OK here, check the transformer primary connections. If you do not get 117 VAC, examine the solder joints on the transformer, fuse block, and interlock switch. If you do get 117 VAC, the problem must be either in the transformer, harness connections, or in the PCB power supply.

If you suspect the transformer, check its secondaries with the VOM set to the 50 VAC scale and correlate the readings with the legend on the side of the transformer. The transformer must also be correctly grounded, so check the ground potential as well, especially if there is a hum bar rolling up or down the Monitor screen.

NO POWER, NO PICTURE — If the Monitor screen is completely dark, first look in back of the Monitor to see if the CRT filament is glowing. If it is, try adjusting the brightness control. If no luck here, put your ear near the Monitor and listen for the high-pitched B+ hum produced by the flyback transformer. If you get the hum but no picture, and you have tried adjusting the brightness, major Monitor servicing is indicated.

If the monitor seems completely dead, check the rest of the game to see if it has power. If it doesn't, go directly to the wall outlet and check there. If OK there, check the game fuse(s), interlock switch, and interconnecting wire lengths.

Sometimes it is difficult to tell if a slow-blow fuse has blown. If in doubt, check it using any of the VOM "R" scales.

HARNESS PROBLEMS — Other harness problems include blowing fuses and malfunctioning controls. The repeating blown-fuse problem can sometimes be quite exasperating to solve. Short circuits have the tendency to occur in areas almost impossible to find. First, try inserting a new fuse as old fuses age and sometimes blow without cause. If the new fuse also blows, you definitely have a short.

The best way to approach this problem is by disconnecting devices that may be causing the problem, such as the TV Monitor, the various PCB's one at a time, and the isolation transformer. Disconnect the devices by **FIRST turning the game off,** disconnecting it from its wall outlet. Remove the blown fuse and connect your VOM across the terminals of the fuse block (this will save blowing a fuse each time you want to check the circuit). Set your VOM to one of its

resistance scales. You should be reading a short. If not, you probably have a part that only shorts out after it is heated up — we'll cover this in a minute. So, assuming you are reading a short on your VOM, disconnect the components from their cabling one at a time, checking the VOM after each one is disconnected. When the short disappears, you have just disconnected the bad component. If all components are disconnected and the short still remains, the problem is in the harness and only patient exploration will reveal its location. Carefully examine all the wiring, looking for terminals that may be touching metal objects such as coins shorting the connections, or burned insulation. If necessary, use the VOM to check each suspected wire.

OK, now let's assume that you connected your VOM across the fuse block terminals as stated above and you did not read a short. This most likely means that you have a component somewhere in that game that **ONLY** goes bad **AFTER** it heats up. It checks good when it's cold. In this case, **turn the game off** and disconnect **ALL** of its components. Install a known good fuse in the fuse block. And turn the game on. If the fuse does not blow after a few minutes, you know that it is not anything to do with the wire harness. (In this instance, it shouldn't be, actually. But it never hurts to check.) Next, **turn the game off again** and reconnect **ONE** component. Turn the game back on and wait a few minutes to see if the fuse blows. If it does not, **turn the game off again** and reconnect another single component. Turn the game back on and wait a few minutes to see if the fuse blows. Repeat this procedure until the fuse blows. When it does blow, the last component you connected has the part on it that is going bad after it warms up and is shorting out.

MALFUNCTIONING CONTROLS — The most common problem here is the bad potentiometer (pot). Typically, a bad pot will cause the image on the screen to jump when it reaches a certain point. The only cure for this one is to install a new pot.

If a feature that is operated by a switch (for example, joysticks, foot pedals, control panel buttons) does not operate at all, check the switch with a VOM or continuity tester to verify its operation. If the switch does not check good, replace it. If the switch is OK, you should suspect the input to the switch from the PCB. In this case, get out the harness and logic schematics and check to see what kind of input is supposed to be at this switch. In many cases, the input will be +5 volts DC. If so, use the VOM to check its presence with the game turned on. Normally, the switch is used to pull a +5 volt DC line LOW to GROUND or to pull a LOW line HIGH. If the PCB output is missing, check the wire length from the PCB. If you find the signal at the PCB trace, the wire length or connection is at fault. If there is no signal at the PCB trace, begin exploring the PCB using the logic schematics and game manual.

MCR II System

The MCR II SYSTEM has four major components: the Linear Power Supply PCB, the CPU Board, the Sound I/O Board, and the Video Generator Board. The manner in which each of these Boards functions and what it does will be explained on an individual basis.

CPU Board — The CPU Board is the main Board of the MCR II System. The other two Boards (Video Generator and Sound I/O) both rely on signals generated by the CPU to enable them to operate. The CPU Board also receives all the voltage requirements for the MCR II System. The signals and voltages required for integrated operation of the CPU, Video Generator, and Sound I/O Boards are transmitted between these Boards via five 24 pin ribbon cables.

The CPU Board can basically be divided into two major sections with regard to the functions it performs:

I. CPU (Central Processing Unit)
II. Background Generator

I. CPU: The CPU section of this Board consists of a Z-80 Microprocessor, operating at 2.5Mhz with 28K bytes of program memory (ROM) and 2K bytes of program RAM. The program memory is stored in seven 2532's, each capable of storing 4K bytes of information. The address boundaries of each program ROM are as follows: 0000 to OFFF is located in ROM 0, 1000 to 1FFF is located in ROM 1, 2000 to 2FFF is located in ROM 2, 3000 to 3FFF is located in ROM 3, 4000 to 4FFF is located in ROM 4, 5000 to 5FFF is located in ROM 5, and 6000 to 6FFF is located in ROM 6. The program ROM selector is 74LS138 which is a 3 to 8 line decoder. It functions as a selector by decoding the addresses from the Z-80 Processor and enabling the proper EPROM to retrieve the data.

The Address Bus of the system has 16 address lines (A0 through A15). These address lines provide the addresses for memory data exchanges and I/O device data exchanges. The Address Bus Buffer consists of two 74LS244's which are Octal Buffers. These Buffers increase the driving capability of the address lines.

The Data Bus has 8 data lines (D0 through D7). This is a bi-directional data bus used for data exchanges with memory and I/O devices. The Data Buffer consists of one 74LS245. The 74LS245 is an Octal Bus Transceiver which provides for communication between Data Buses.

The Control Bus is made up of 6 control lines coming from the Z-80 Processor. These signals are: $\overline{M1}$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RFSH}$. These signals help control the sequence of events during operation of the system. The Control Buffer consists of one 74LS367, a Hex Bus Driver. This device also helps improve the drive capability of the control lines.

Interrupts on the CPU are handled through the CTC (Counter Timer Circuit). The CTC receives a 493 signal which indicates we are at the bottom of the screen during scan time. The CTC then triggers a timer which will generate an interrupt 1.2ms later. During this time (1.2ms), background, color registers, coin counters, and game sounds are serviced.

One feature on the CPU Board is the WATCH-DOG. This is a 74161, a Binary Counter. This device is set up to count from "0" to "15". Every 32ms while the game program is running the Watch-Dog receives a "clear pulse". If the game program gets lost, the Watch-Dog will not receive a "clear pulse" and will reset the system.

The CPU Board also has a Non-Volatile RAM which is part of the Battery Backup System. This RAM will store information in case of a power failure or when the game is turned off for any reason. With the Battery Backup System special consideration had to be taken during the power up and power down sequence in order to preserve the data in the N-V RAM. During power up you have to guarantee that the chip select to the N-V RAM is pulled up high. And during power down you want to delay the reset pulse until all writing to the N-V RAM has been completed. These conditions are met by the circuitry of the Custom Control Chip with the 4017 and 4053.

II. BACKGROUND GENERATOR: The Background Generator section of the CPU Board is made up of a 32 byte block by 32 byte block array. Each block of the array can be individually specified by the programmer. An individual block can be broken down to 8 pixels by 8 pixels. Each pixel is composed of 4 bits. So, one 32 byte block is equivalent to 256 bits of information.

The main function of the Background Generator is to take the background information and multiplex it with the foreground information to determine which video information is to be displayed.

In the Background circuit there is a 1K by 8 RAM which contains a description of the 32 by 32 array. There is a one to one correspondence between the blocks as they appear on the screen and their corresponding RAM locations. Each byte of data in the RAM is a pointer to the picture that is to be displayed in that block. The address lines going to the RAM come from a two to one Multiplexer.

The Multiplexer selects between the Microprocessor Address Bus or Horizontal Counters H4 through H8 and Vertical Counters V3 through V7. The lower order horizontal and vertical counter bits are not needed for addressing the Background RAM. If the Background RAM needs updating, the Multiplexer would select the Microprocessor Address Bus via the Z-80. Miscellaneous odd bits of video will appear on the monitor screen if the Microprocessor updates the RAM anytime other than Vertical Blanking.

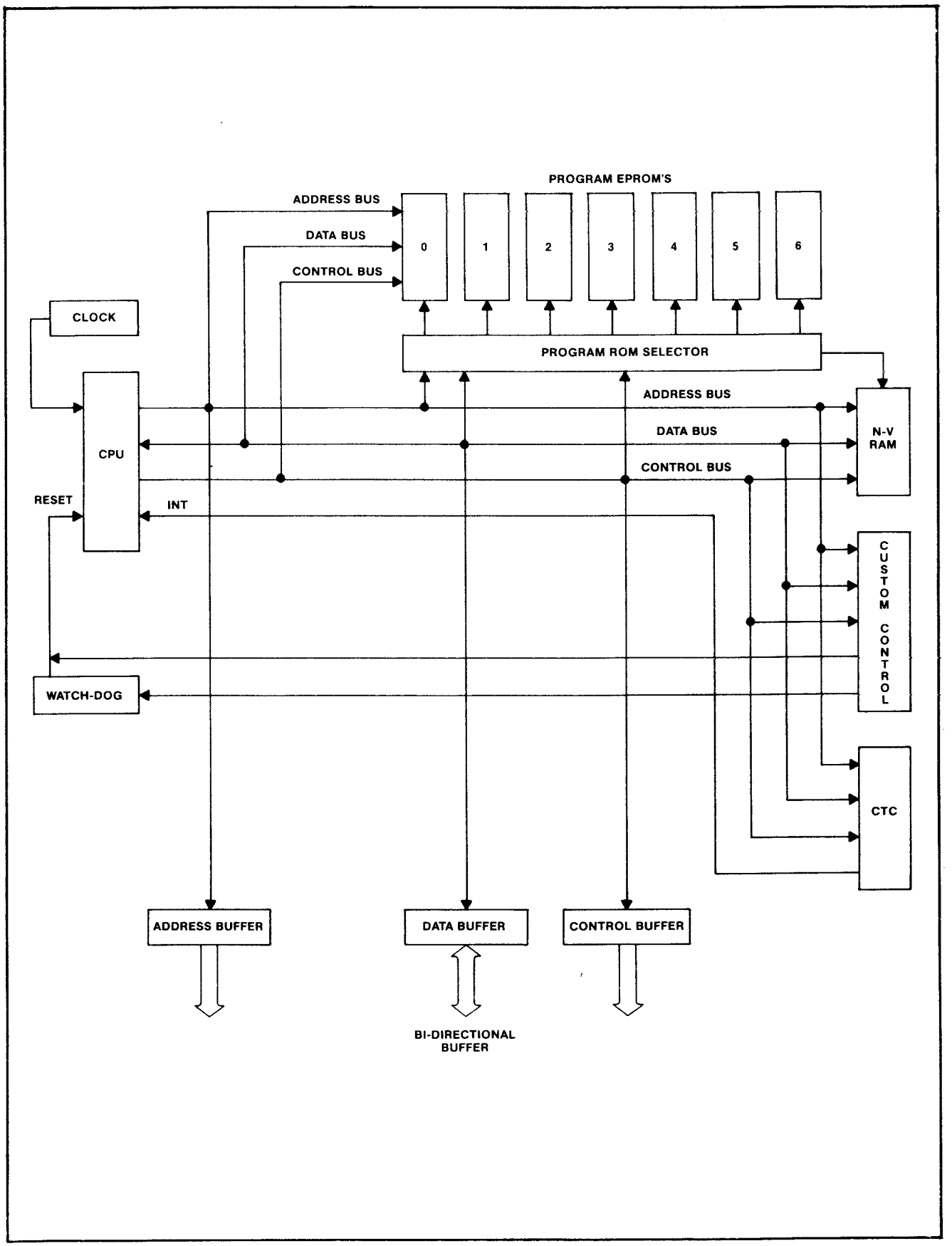
During game play, the Multiplexer has the Horizontal and Vertical Counters selected. This insures that the address lines to the RAM change only 32 times during a horizontal line and 32 times for a vertical scan. Whenever the count is within the boundaries of a block, the same 8 bits of data appears at the output of the RAM. These 8 bits of data from the RAM are now latched by the 74LS374. This latched data now becomes the upper address lines to two 2732 EPROM's. The lower order address lines consist of H3, a Horizontal Counter signal **AND** DV 0 through DV 2, Vertical Counter signals. These signals complete the addressing to the EPROMS. The upper address addresses **BLOCK BOUNDARIES** and the lower address addresses the data **WITHIN** the block boundaries.

So, for one block's worth of scan time, the upper order address lines remain fixed while the lower order lines count out the individual bytes. The 8 bits of data out of each of the EPROMS is latched again by two 74LS374's. This information is next fed to two 74LS153's which are four to one Multiplexers. These Multiplexers perform the function of converting the 8 bits of data into two 2 bit data streams. The multiplexing is controlled by H1 and H2 from the Horizontal Counters. The two 2 bit data streams are now joined together and represent 4 bits of data, the equivalent of one pixel's worth of information.

These 4 bits of background information and 4 bits of foreground information are both now fed into a 74LS157, a 2 to 1 Multiplexer. This Multiplexer acts as a switch in the sense that it selects between either foreground or background information to be displayed.

The control for the 74LS157 is a 7427 which acts as a Detector. If the 7427 detects foreground information, a signal is sent to the 2 to 1 Multiplexer by it causing only foreground information to pass through. At all other times, background information is allowed to pass through. The signal from the Detector is also used to select between the Foregound Color RAM or the Background Color RAM.

The 4 bits of data out of the 2 to 1 Multiplexer, being either foreground or background information, is again fed to another 2 to 1 Multiplexer with A0 through A3. This Multiplexer can select between video information and CPU address A0 through A3. This multiplexed data now becomes an address to the Color RAM. The Color RAM consists of 6 fast Bipolar Static RAMS, 4 by 16 bits each.



CPU BLOCK DIAGRAM

The Color RAM is set up into three pairs of RAMs representing RED, GREEN, and BLUE. In each of the pairs, one RAM is for background and the other is for foreground information. Each Color RAM has the ability to generate 16 shades of color. So the system is capable of generating 4096 different colors, sixteen of which may be displayed on the screen at any one time. As the data in the foreground/background combination changes, different locations are addressed in the Color RAMS, and corresponding data is outputted by the Color RAMs. The data out of the Color RAMs is converted to voltage levels using a Resistor Network and a Current Mirror. These are then interfaced to a color CRT.

SUPER CPU BOARD — The Super CPU Board is very similar to the CPU Board previously described. The foreground board is unchanged. And the I/O Port locations and the foreground memory location remain unchanged. However, the background RAM, the color RAM, and the CPU RAM have been changed.

BACKGROUND RAM: There are still 32 x 30 blocks visible on the monitor screen. However, now two bytes are being used to define a block. The "word" defining a block is stored with the least significant byte first. The least significant nine bits (bits 0 through 8) define the picture number. This makes it possible to address 512 pictures directly. Bit 9 controls the horizontal flipping of the picture (when bit 9 is equal to Logic "0", the picture is UNFLIPPED and when bit 9 is equal to Logic "1", the picture is FLIPPED). Bit 10 controls the vertical flipping using the same principal stated above for the horizontal circuit. Bits 11 and 12 define the color group of the picture. There are 64 colors that may be displayed. These are divided into 4 groups of 16 colors each. The color group number defines which of the 4 groups the picture belongs to. Therefore, it is possible to display the same picture in different colors. Bit 13 is not used. Bits 14 and 15 define the color group a foreground object will fall into when it passes over that square. In this way, it is possible to sectorize the screen so that a single foreground picture has more than one set of colors depending on its location on the monitor screen. Simply equating these two bits (14 and 15) to zero will make the foreground video identical to that produced by the older version of this system.

The background video RAM is located at F800H through FF7FH. There are 1920 memory locations because there are 32 x 30 blocks and each block is defined by two bytes.

COLOR RAM: The color RAM is arranged 64 x 9 bits. There are 64 colors, each of which is 9 bits wide. Therefore there is a possibility of 512 different colors ($2^9 = 512$), any 64 of which may be displayed. These 64 colors are shared by both background and foreground video. Each one of the color registers is located at a "word" boundary. The lower 8 bits of the color registers are equivalent to D0 through D7. The most significant bit of the color register is addressed by A0. The color RAM is located at FF80H through FFFFH.

To write the number 155H to color register 10H, you would have to write 55H to location FF80H + (10H x 2) + 1.

- FF80H represents base location.
- 10H x 2 represents register 10H at 2 bytes per register.
- 1 because the most significant bit of the register is set. Therefore A0 = 1.

To write 055H to the same register, you would have to write 55H to location FF80H + (10 x 2).

Each color gun of the picture tube is controlled by 3 bits of a color register. Bits 0 through 2 control green, bits 3 through 5 control blue, and bits 6 through 8 control red.

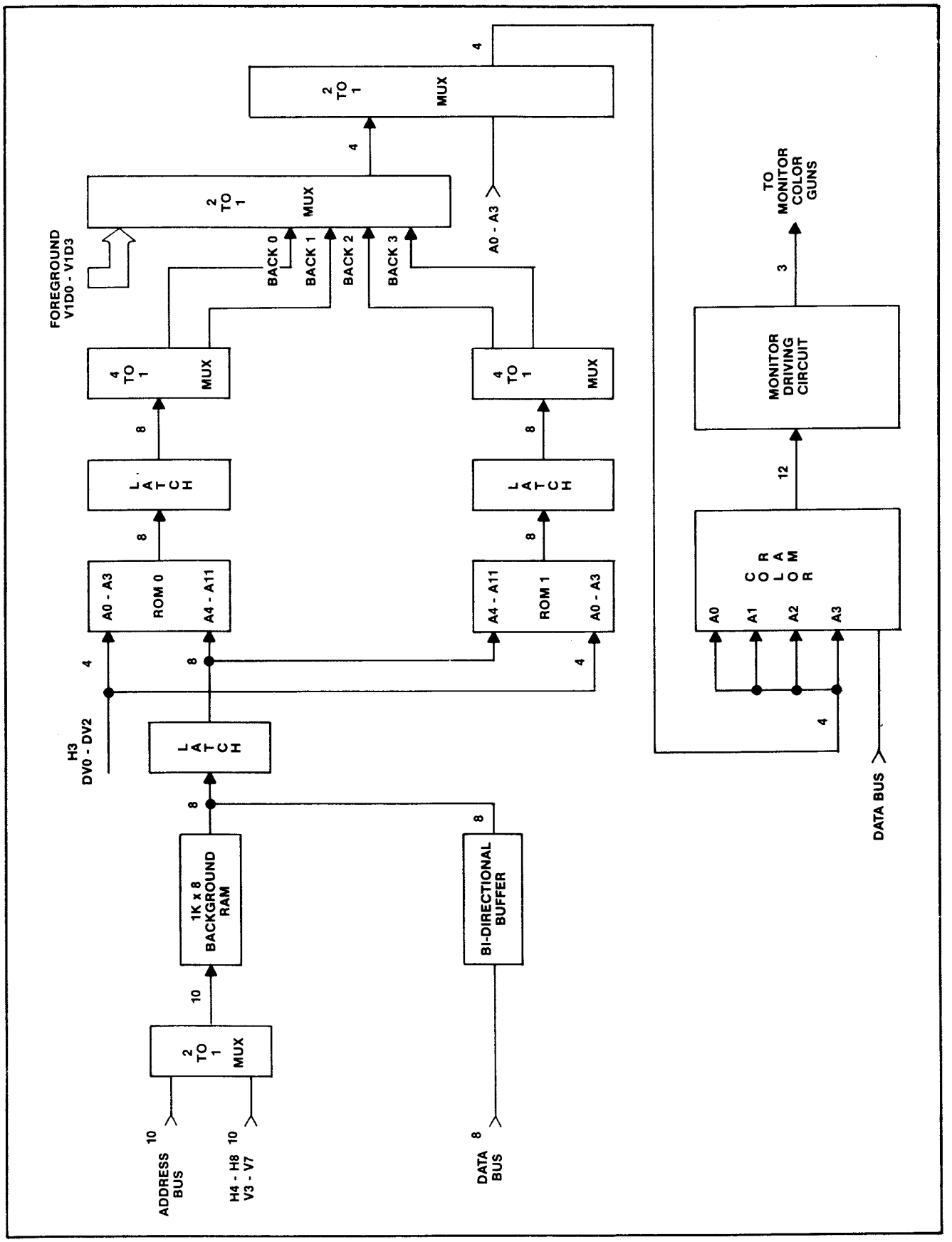
CPU RAM: The CPU RAM is now located at C000H through C7FFH. This is the only change here.

VIDEO GENERATOR BOARD — The Video Generator Board was designed to display video images on a CRT Monitor Screen. This PC Board is controlled by the Microprocessor on the CPU Board. The Microprocessor specifies **EXACTLY** which images are to be displayed. It also specifies the **EXACT** physical location on the Monitor Screen where **EACH** of those images is to be displayed. The hardware on the Video Generator Board then uses this information to construct the images for the whole Monitor Screen.

DOUBLE LINE BUFFER: OVERVIEW The Double Line Buffer is a video display consisting of 128 individual, independent objects — later referred to as the "foreground".

The basic principle for the foreground of the system is that there are two RAM Buffers. Each RAM Buffer is capable of holding one scan line worth of information. The Buffers compliment each other in their functioning. While one Buffer is unloading (dumping) its information to the Screen, the other Buffer is loaded with data for the next scan line. When the next scan line comes around, the Buffer that has just been loaded dumps its data to the Screen, while the one that had been dumping is now loaded with new data.

The display resolution is currently 512 pixels per horizontal line and there are 479 interlaced lines.



BACKGROUND BLOCK DIAGRAM

DETAILED DESCRIPTION There is a system clock which runs a 10 bit Horizontal Counter. The Horizontal Counter counts from 0 to 511 during active scan time and from 512 to 634 during horizontal retrace. Once a count of 634 is reached, the Counter is reset to zero. Each time a count of 512 is reached, the Vertical Counter is incremented. This is a full interlace system. The Vertical Counter starts at 0 and counts to 239.5 during active video. There are only 16 lines of retrace and the second frame starts on a count of 255.5. Active video occurs up to a count of 495. Then there are 16 lines of retrace again. On a count of 511, the Vertical Counter is reset to zero. The half line count is obtained by detecting the mid-point of the horizontal count.

The Object RAM contains the data about each of the 128 foreground objects. The Object Address Counter is the 9 bit Counter that provides the address lines which step through the Object RAM locations. This Counter is set to zero at the start of every horizontal scan line. In the Object RAM, there are 128 object packages. Each object package has 4 bytes associated with it. The 1st byte of the package contains the vertical position, the 2nd byte contains the picture number, the 3rd byte contains the horizontal position, and the 4th byte is a blank byte which may be used by the programmer as some form of status byte. The 4th byte **DOES NOT** affect the displayed image in any way.

The Object Address Counters start the first object package and count in steps of 4, i.e., they look at the vertical position of the packages to determine whether an object is to be loaded into the Buffer for this particular scan line. The method by which it is determined whether an object is to go into the Buffer or not is this: The vertical position is added to the Vertical Counter and the result latched. If there are all 1's in the most significant 4 bits, then the object is loaded into the Buffer. The Vertical Counter is a 9 bit Counter with the most significant bit representing the frame number (odd or even frame). So, for any given frame, it is effectively an 8 bit Counter. The Vertical Counter starts at zero at the top of the screen. The vertical position specified uses a coordinate system of zero on the bottom. When the two 8 bit quantities are added, all 1's will occur in the most significant 4 bits 16 scan lines before the sum is all 1's in all 8 bits. This condition occurs 16 times in the odd frame and 16 times in the even frame which makes up a single object 32 lines in height. The upper 4 bits of the sum go to the ROM address lines A3 through A6 while the lower 4 bits increment every horizontal line so they are used to address successive lines of the picture in the ROM.

The Counter Control Circuit is used to control the frequency and increment amount of the Object Address Counters. At the start of every horizontal scan time, the Control Circuit ensures that the Object Address Counters count in steps of 4 and at a rate of 200 nanoseconds.

When it is determined that an object has to be loaded into the Buffer, the Control Circuit switches the count sequence to steps of 1 so that successive bytes of data may be retrieved from the Object RAM. At the same time, the counting rate is slowed to 800 nanoseconds. This reduced counting speed is required because it takes time for an object to be loaded into the Buffer. If the counting rate were not slowed down, the hardware might attempt loading a second object into the Buffer before the first was completed. Once an object has been loaded into the Buffer, the counting rate goes back to 200 nanoseconds and the counting back to steps of 4.

Once it has been determined that an object is to be loaded into a Buffer, the Object Address Counter begins counting in steps of 1. The next byte that comes out of the Object RAM is the picture number. This is latched into the Picture Latch. The picture number now becomes the upper address lines to the ROMs. These upper address lines point to the block of memory where that particular picture is stored. A Byte Counter is initiated when the picture number is latched. This Byte Counter counts out the bytes in one horizontal line of the picture stored in the ROMs. This allows successive bytes of information to be sent to the Buffers.

After the picture number is latched, the Address Counters pick out the horizontal position byte. This information is loaded into an 8 bit Counter. This Counter is labeled Buffer Loading Counter. The data from the ROMs is pulled out 32 bits at a time. These 32 bits are loaded into the Shift Registers. The Shift Resisters shift out data at the same rate as the Buffer Loading Counter is counting. By this means, picture information from the ROM is loaded into successive Buffer locations starting at the location specified by the horizontal position byte. The Shift Registers shift out 32 bits of data, 8 bits at a time. When the next 32 bits have been shifted out to the Buffer, the Byte Counter to the ROMs increments and the next 32 bits is loaded into the Shift Registers. This process is done a total of 4 times for one horizontal line of a single object and a total of 128 bits of data are sent to the Buffer. Each pixel is composed of 4 bits, so there are 32 pixels in a horizontal line of a picture.

During each data load cycle into the Buffer, data already existing in the Buffer is first read out, "OR"ed with the incoming data. The result of the "OR"ing is latched, and then read back into the Buffer. The "OR"ing operation is performed to insure that the picture background information, which consists of all zeros, does not erase data already existing in the Buffer.

When it is time to output the data from the Buffer, the Buffer Multiplexers switch the Buffer Address Lines to the Horizontal Counters. Data coming out of the Buffer RAMs is latched into the Data Out Latch. After data has been read out of each byte of the Buffer RAM, zeros are written into each location. This

clearing of the Buffer RAM is accomplished by holding the "data-in" inputs to the Buffer RAM at all zeros and providing a write signal. This flushing operation is necessary because the Buffer has to be cleared of old data (previous horizontal line) before new data (upcoming horizontal line) can be entered.

Data coming out of the Buffer is 8 bits wide. A 4 bit 2 to 1 Multiplexer is used to provide a stream of data 4 bits wide. This Multiplexer switches between the 2 sets of 4 bits at the pixel rate.

The Staging RAM is the RAM into which the controlling CPU (usually Microprocessor based) reads and writes. Every 1/30th of a second, data is moved from the Staging RAM to the Object RAM. This is done during every second vertical blanking time. The total move takes 8 horizontal line times or 508 microseconds. During the move time, the Multiplexers to the Staging RAM allow the Transfer Counters to go through the RAMs. At the same time, the Multiplexers to the Object RAM allow the same Counters to go to the Object RAM. These Counters step through successive locations in the Staging RAM and the data from these RAMs is presented at the inputs to the Object RAM. A write enable signal is generated and sent to the Object RAM for each address. Since the Address Lines to each of the RAMs is identical, data is transferred from the Staging RAM to the Object RAM. When the data transfer is complete, the Multiplexers switch and allow the Microprocessor Address Bus to get to the Staging RAM and the Object RAM Multiplexers allow the Object Address Counters to get through to the Object RAM. The Transfer Counters are nothing but a combination of the Horizontal and Vertical Counters, H3 through H8 and V0 through V2.

SOUND I/O BOARD — The Sound I/O Board handles all sound generation and game control input and output. This Board's functions can be divided into two major catagories:

I. Sound Generator and Controller.
II. Main CPU Input and Output.

I. SOUND GENERATOR AND CONTROLLER: GENERAL DESCRIPTION The Sound Generator and Controller is a microprocessor controlled system which generates filtered square waves for use in video games. The system generates sounds upon request from the main CPU on the CPU/Background Generator Board. There are six channels of square waves and/or noise which are the inputs for six programable low pass filters. The filters are then summed together in groups of three to form two channels, each of which can be panned from left to right. The outputs of the panning circuits are preamplified for use as inputs to the power amplifiers located elsewhere in the game.

DETAILED DESCRIPTION The Sound Controller consists of a Z80 microprocessor operating at 2MHz with 16K bytes of program memory (ROM) and 1K byte of program RAM. The program memory is stored in four 2532's, each of which is capable of storing 4K bytes of information. The address boundaries for each program ROM are as follows: 0000 to 0FFF is located in ROM 0, 1000 to 1FFF is located in ROM 1, 2000 to 2FFF is located in ROM 2, and 3000 to 3FFF is located in ROM 3. The program ROM selector is a 74LS138, which is a 3 to 8 line decoder (located at B12 on the Board). It functions as a selector by decoding the addresses from the Z80 microprocessor, enabling the proper ROM to retrieve the data.

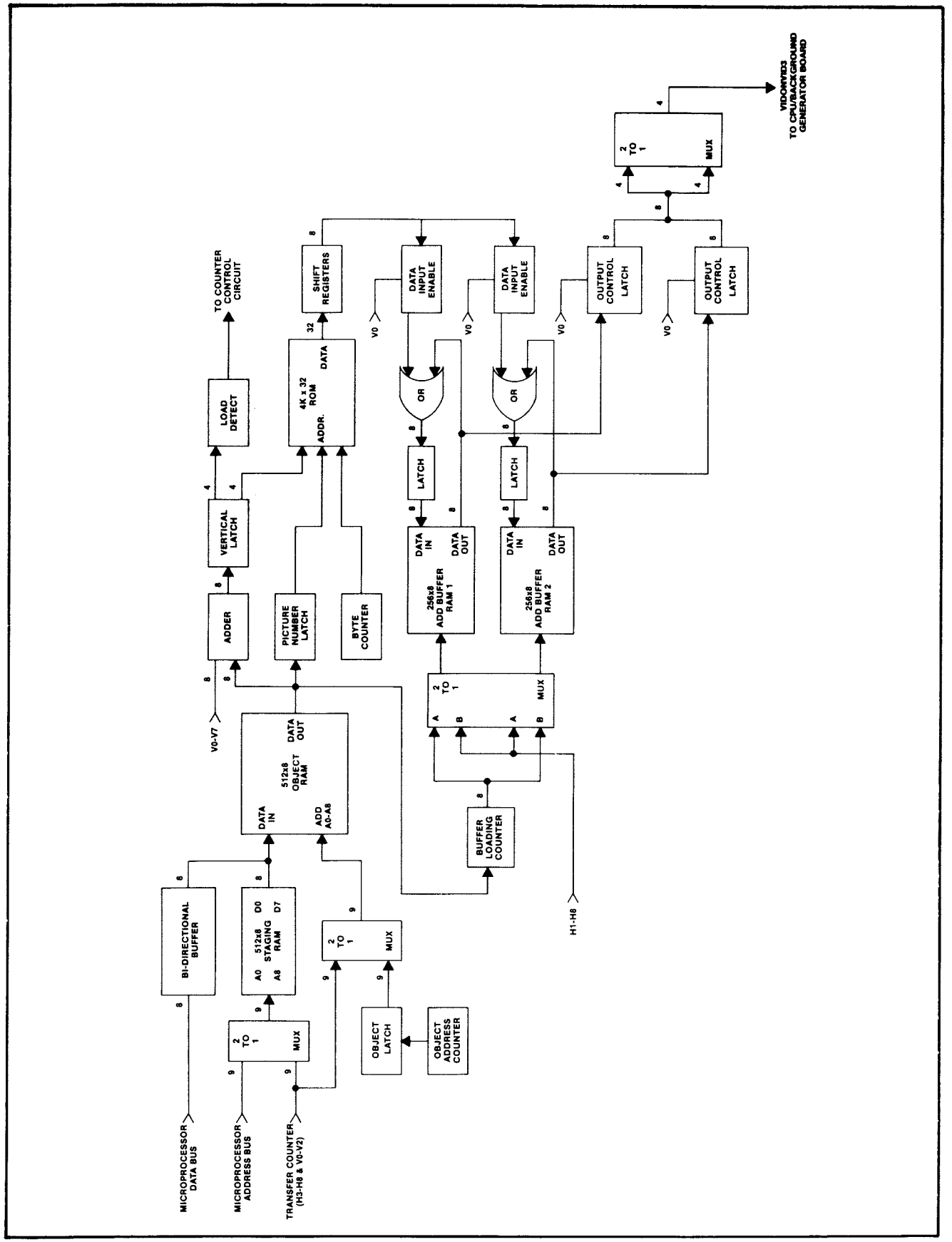
The address bus of the system has 16 address lines (A0 through A15). These address lines provide the addresses for memory data exchange and peripheral data exchange.

The data bus has 8 data lines (D0 through D7). This is a bidirectional data bus used for data exchange with memory and peripheral addresses. The data bus buffer consists of one 74LS245. This 74LS245 is an octal bus transceiver which provides for communication between data buses.

Control of the memory and Peripherals is provided by RD, WR, MREQ, and RFSH control lines. These signals help control the sequence of events during operation of the sound system. The signals are used in conjunction with the address bus and the 74LS138's (located at B12 and B13) to provide select pulses to the components of the Sound Controller.

In order to keep track of all the control signals used on the Sound I/O Board, certain fixes are used for the CPU signals. A $\underline{u}$ is used to indicate an unbuffered signal to or from the main CPU on the CPU/Background Generator Board. A $\underline{Bu}$ is used to indicate a buffered signal to or from the main CPU on the CPU/Background Generator Board. An $\underline{s}$ is used to indicate an unbuffered signal to or from the Sound CPU. A $\underline{Bs}$ is used to indicate a buffered signal to or from the Sound CPU.

The Sound Generator is composed of two AY-3-8910's (Programable Sound Generators). Each AY-3-8910 is a large scale integrated circuit that can produce a variety of sounds under control of the sound CPU. Each of the above chips produces three channels of analog output. Each of these three channels is connected to a duty cycle controlled low pass filter. There are six of these low pass filters in all. Each is under the control of the Sound CPU. They are used to color noise outputs, removing varying degrees of harmonic contents from square wave outputs, providing a range of different tone qualities, or to provide fairly low distortion sine waves for purposes of additive synthesis. The filter outputs are summed into groups of three to yield two channels of sound. These two channels can be panned, or moved, from the left preamp to the right preamp or to a place between the left and right channels. The preamps drive the power amps. Each section is described below.


MICROPROCESSOR DATA BUS
MICROPROCESSOR ADDRESS BUS
TRANSFER COUNTER (H3-H8 & V0-V2)
BI-DIRECTIONAL BUFFER
512x8 STAGING RAM
A0
A8
D0
D7
2 TO 1 MUX
OBJECT LATCH
OBJECT ADDRESS COUNTER
2 TO 1 MUX
512x8 OBJECT RAM
DATA IN
ADD A0-A8
DATA OUT
V0-V7
ADDER
PICTURE NUMBER LATCH
BYTE COUNTER
VERTICAL LATCH
LOAD DETECT
TO COUNTER CONTROL CIRCUIT
4K x 32 ROM
ADDR.
DATA
SHIFT REGISTERS
BUFFER LOADING COUNTER
H1-H8
2 TO 1 MUX
A
B
DATA IN
DATA OUT
256x8 ADD BUFFER RAM 1
256x8 ADD BUFFER RAM 2
LATCH
OR
DATA INPUT ENABLE
V0
OUTPUT CONTROL LATCH
2 TO 1 MUX
V0-V3
TO CPU/BACKGROUND GENERATOR BOARD

The AY-3-8910 PSG's provide three analog channels of output and 16 bits of digital output each. The PSG's are written to under control of the Sound CPU. The PSG chip selects are provided by the 74LS138 located at B13. The digital outputs of the AY-3-8910's are used to select the filter values for the low pass filters, the panning information for the panners, and the sound on bit for the preamplifiers.

The duty cycle controlled low pass filters allow programable low pass filtering of the analog information. Each filter can be set to select 1 of 16 filter frequencies out of a range between 330Hz to 13KHz. A four bit number from the appropriate output port determines which of the 16 cut-off's is chosen. The four bit number is periodically loaded into the filter control counter. With counter clock signal the counter counts down until it reaches "0", at which time the terminal count signal goes high. If the counter is preloaded with a zero, the terminal count goes high immediately and stays high the whole time. This provides a duty cycle of 100% and sets the cut-off of the filter to the highest frequency. If it is preloaded with a large number, the terminal count will be low for part of the cycle. This provides a duty cycle of less than 100% and sets the cut-off of the filter to a lower frequency. This is accomplished by letting the terminal count control an analog switch in series with a resistor in the opamp filter circuit. This effectively varies the value of the resistor by only letting it conduct for a fraction of the time. This varies the cut-off frequency as the effective resistance varies.

In order to be able to tune the filters over a wide frequency range and to have the cut-off frequencies separated by equal frequency ratios, an exponential series of clock pulses is used to clock the 6 filter control counters. This exponential clock is generated by a four bit binary counter connected to a four bit BCD decade counter to form a ROM address counter. This ROM address counter is clocked at 8MHz and continuously counts from zero to 159 and rolls over. This happens at a 50KHz rate. Each time the ROM address counter rolls over, a signal is given which loads the preload number from the Sound Generators to the filter control counters. The five highest lines of the ROM address counter are used to step through the first twenty locations of the 32 x 8 exponential pattern ROM. The three low order lines of the ROM address counter go to a load detect circuit which latches the output of the exponential pattern ROM into the shift register when these three lines are all low. The used portion of the exponential pattern ROM in conjunction with the eight bit parallel to serial shift register form in effect a 160 x 1 serial ROM. The output of the shift register is gated with an 8MHz clock signal and used to clock the filter control counters. The exponential ROM is programed with all ones except for 15 bits which are zeroes. These 15 bits are spaced in such a way that the ratio of the quantity 160 minus the bit number (0 through 159) for two adjacent "ON" bits will be approximately equal for any two adjacent "ON" bits. In this way, the cut-off frequencies of the low pass filters are exponentially spaced, which corresponds to the exponential nature of sound perception.

The three filtered signals from each PSG are summed together and low pass filtered at 18KHz to remove the 50KHz duty cycle modulation switching noise. Each of the two resultant signals go to an analog multiplexer which is used with a resistor network to control apparent placement of the sound from left to right. Each analog multiplexer is controlled by three bits of digital output from a port on its associated PSG.

The two left channel signals are summed and amplified by the left preamplifier. Similarly, the two right channel signals are summed and amplified by the right preamplifier. Each preamplifier is also a low pass filter set at 18KHz to provide additional filtering of the 50KHz duty cycle modulation switching noise. The preamplifiers are current input (Norton) type 3900 op amplifiers. The panning outputs are converted to current by the large input resistors. The sound is turned off by forcing additional current into the op amp input. This forces the preamp output high, thereby turning the sound off. The volume control is handled in a similar way. The volume control is a pot located off board and generates a control voltage. This control voltage is converted to a current which is subtracted from the preamps input. When enough current is subtracted, the gain is very low. When no current is subtracted, the gain is normal.

The main CPU interfaces to the sound CPU through two means. The interface RAM (locations B9 and B11) provides 4 - 8 bit bytes that the main CPU can only write to, and the sound CPU can only read. In this method, the main CPU makes sound requests to the sound CPU. There is a status port (located at A5) that is an 8 bit byte that the sound CPU can only write to and the main CPU can only read. This provides status information that can be read back by the main CPU.

In order to generate accurate sounds, there is a 1.28ms interrupt timer that is used to provide accurate time intervals to the sound CPU. A 4024 seven stage ripple-carry binary counter is used to divide down a 50KHz clock to 391Hz. This would appear to be a 2.56ms signal. However, each time the output of the counter goes high, the CPU manually resets it to clear the interrupt. Since this goes high at half the time rate, the interrupts occur every 1.28ms. A pulse from the 74LS138 (B13) is used to clear this counter under CPU counter.

The sound CPU also has an 8 bit dip switch (located at D14) of which the first 6 bits are used as an input port to the sound CPU. With this dip switch board level tests can be requested. A yellow LED is also connected to an output port in order to provide a means to report sound CPU test results when a test is requested via the dip switch. Both of these input and output ports are selected by the 74LS138 (B13).

II. MAIN CPU INPUT AND OUTPUT — The I/O section of this PCB contains the port decoding circuitry and the input and output buffers for the main CPU (which is located on the CPU Background Generator Board).

There are two 74LS138's which do the port decoding to enable an input or an output. The 74LS138 at B7 decodes the input ports and decides whether one of the three RRC switch inputs, two dip switch inputs, or the sound CPU status port is being addressed. The 74LS138 at B8 decodes the output ports and decides whether one of dedicated output ports (coin counters and video flip bit), the miscellaneous output port, or the interface RAM to the Sound Board is being addressed.

The three RRC (resistor, resistor, capacitor) input ports are external inputs such as coin switches. The switch information enters into the Board by the right angle edge connectors. Each input bit is filtered with a resistor and a capacitor and then pulled up with a second resistor.

Each RRC filter output goes into the input to a 74LS244 buffer. The 74LS244, when selected by the 74LS138 address decoder, allows the RRC input information at its input to be placed upon the Bu data bus where the main CPU can read it. There are currently three such 74LS244's and RRC filters currently providing 24 bits of input.

There are two banks of dip switch inputs (located at B3 and B6) which are used to set options for the main CPU. Each switch output is tied high via a pull up resistor and used as an input to a 74LS244 buffer. The 74LS244, when selected by the 74LS138 address decoder allows the dip switch information to be placed upon the Bu data bus where the main CPU can read it. There are two such 74LS244's providing 12 bits of dip switch input. (Note: On some later versions of this Board, one dip switch (dip sw 2) will be deleted and an extra RRC input port will be added.) Dip switch 1 is special in that it has 10 positions. Position #9 is not used. Position #10 is used to ground the u wait line. This causes the main CPU to go into continuous wait states. This will freeze the main CPU causing the video to be static and allow easier troubleshooting of video section. (Note: This will not freeze the Sound CPU. Any sound in progress will go as far as possible to completion.)

There is a 74LS374 eight bit latch with tristate outputs that is used as a status port from the Sound Board. The sound CPU writes information onto this latch. The main CPU can enable the output of the latch with a signal from the 74LS138 causing the information to be placed on the Bu data bus and allowing the main CPU to read the status port.

The sound interface RAM is 4 bytes of ROM that the main CPU can write to and the sound CPU can read. The 74LS138 is used to select the interface RAM and to store the data off of the Bu data bus into the interface RAM.

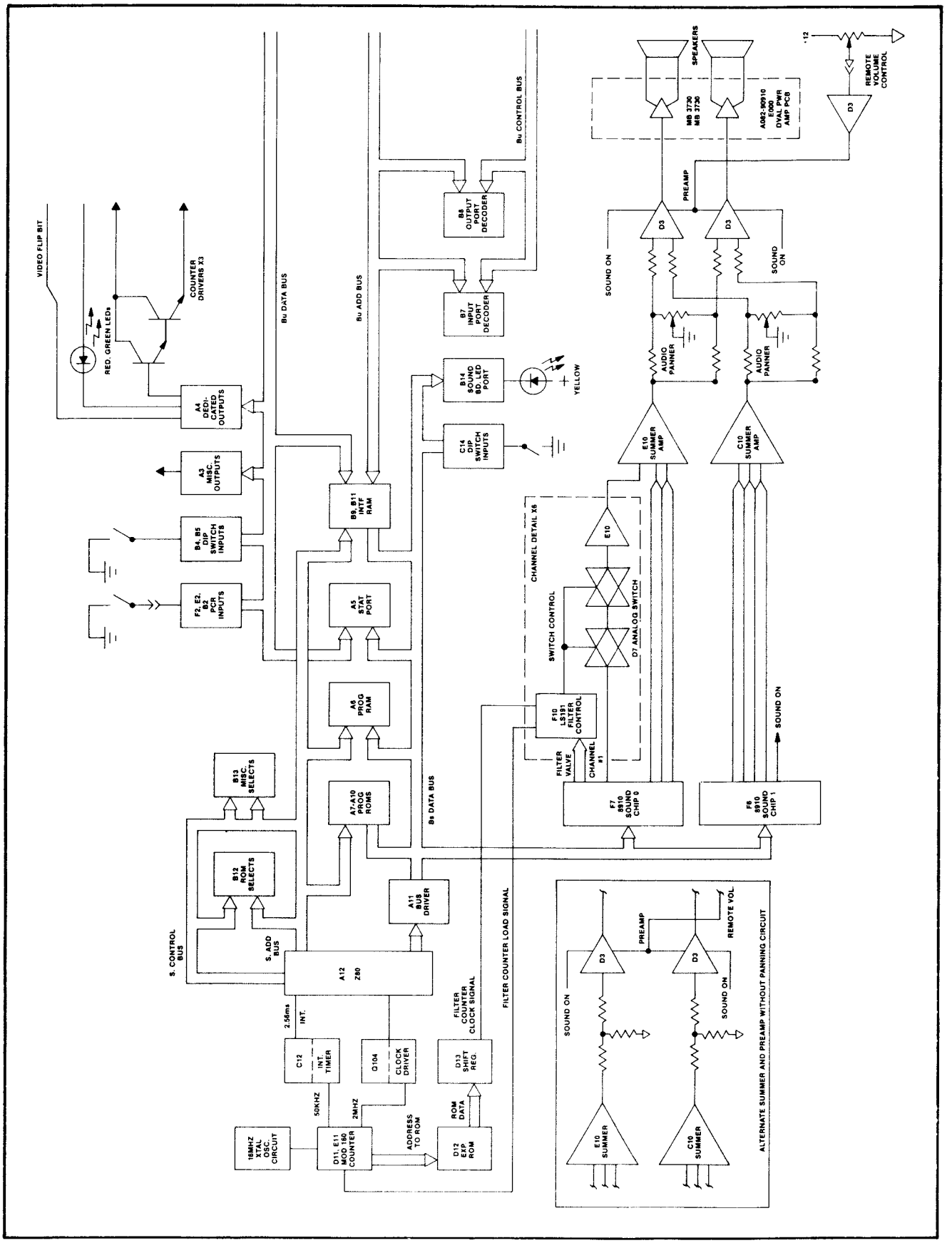
There are two 74LS273 eight bit latches that are used as output ports. They can be individually selected by the 74LS138 and have the data on the Bu data bus strobed into their inputs. The latch at A3 is used for miscellaneous outputs and goes off the Board via the right angle edge connector. The latch at D4 is used for dedicated outputs. This includes three high current open collector transistor outputs for use in driving coin meters, one bit for video chip line used for screen flipping in Cocktail Table games, and for enabling a red or green LED used for test purposes.

SUPER SOUND I/O BOARD — The Super Sound I/O Board is very similar to the Sound I/O Board previously described. The differences are two fold:

1. Dip switch 2 has been deleted and another RRC input port added in its place. This RRC input port uses the 8 bits previously used by dip switch 2 and 1 bit from dip switch 1. This provides a total of 33 bits of input for the system.
2. The panning circuitry has been deleted. The outputs of the left and right summing amplifiers now go directly to their respective pre-amplifiers.

POWER SUPPLY BOARD — INTRODUCTION: This Power Supply Printed Circuit Board (PCB) assembly has been designed in such a way that it can be used for all games of the MCR II series and Vector Scan Systems. Although some games do not draw the full amount of power these supplies are capable of generating, there are others that do. So, the supply was designed to operate the biggest power hog. This Power Supply PCB generates quite a few different voltages, both regulated and unregulated, which are used to operate a number of different types of componentry. The +5V and +12V supplies are high current sources carefully regulated by a standard fold-back current-limited circuit design which compensates for both line voltage and load fluctuations, and prevents burn-out due to an overload or shorted circuitry. In addition to the regulated supplies, two unregulated supplies are also incorporated to power incandescent lamps and audio circuitry.

SENSE AND COM. LINES: One interesting feature of the power PCB is the use of the SENSE and COM. LINES to detect any IR drop which might occur in the ground line between the power PCB and the CPU PCB. IR drops across a ground line can cause several problems, including the annoying hum bar which rolls up the monitor screen infuriating operators and players alike. Essentially, both the SENSE and COM. LINES are connected together just after they enter the CPU PCB. Because the SENSE LINE is connected to the COM. LINE at this point, it can be used to detect any IR drop which might occur between the power PCB and the CPU PCB. And, because the SENSE LINE is used as the COM. reference for the entire power PCB, any IR drop which occurs across the COM. LINES simply offsets the entire power supply system by that amount and thereby eliminates


VIDEO FLIP BIT
RED, GREEN LEDs
COUNTER DRIVERS X3
Bu DATA BUS
Bu ADD BUS
Bu CONTROL BUS
B8 OUTPUT PORT DECODER
B7 INPUT PORT DECODER
B14 SOUND BD. LED PORT
YELLOW
C14 DIP SWITCH INPUTS
A4 DEDI-CATED OUTPUTS
A3 MISC. OUTPUTS
B4, B5 DIP SWITCH INPUTS
F2, E2, B2 PCB INPUTS
B9, B11 INTF RAM
A5 STAT PORT
A6 PROG RAM
A7-A10 PROG ROMS
B13 MISC. SELECTS
B12 ROM SELECTS
A11 BUS DRIVER
A12 Z80
S. CONTROL BUS
S. ADD BUS
8x DATA BUS
2.56ms INT.
C12 INT. TIMER
50KHZ
C104 CLOCK DRIVER
2MHZ
D13 SHIFT REG.
FILTER COUNTER CLOCK SIGNAL
FILTER COUNTER LOAD SIGNAL
ROM DATA
ADDRESS TO ROM
18MHZ XTAL OSC. CIRCUIT
D11, E11 MOD 180 COUNTER
D12 EXP ROM
CHANNEL DETAIL X6
SWITCH CONTROL
D7 ANALOG SWITCH
E10
F10 LS191 FILTER CONTROL
FILTER VALVE
CHANNEL #1
F7 8910 SOUND CHIP 0
F8 8910 SOUND CHIP 1
SOUND ON
E10 SUMMER AMP
C10 SUMMER AMP
AUDIO PANNER
PREAMP
D3
SOUND ON
MB 3730
MB 3730
A082-90910 E000 DVAL PWR AMP PCB
SPEAKERS
REMOTE VOLUME CONTROL
ALTERNATE SUMMER AND PREAMP WITHOUT PANNING CIRCUIT
REMOTE VOL
E10 SUMMER
C10 SUMMER

any problematic conditions which might otherwise occur. Commonly, only the SENSE LINE for the +5V is used, and the SENSE LINE for the +12V is then connected to it with jumper JW2. In cases where more than 2 Amps is sourced by the +12V supply, it may be desirable that the +12V supply use its own SENSE LINE, in which case jumper JW2 is deleted.

Jumpers JW1 and JW3 can be used to control hum in the audio. Their only justified use is when there is a considerable distance between the Filter Assembly and the Power Supply PCB. Another option to control this hum is by connecting the SENSE LINE(S) to the filter assembly via pins 7 and/or 9 of connector J3.

THE TRANSFORMERS: The Game Logic Transformer is unique in the video game industry because it doesn't have taps to compensate for high or low voltage. It is a constant-voltage transformer which adapts itself automatically to line voltage variations and fluctuations. The output voltages stay constant with line voltage variations from 100 to 125VAC (MT00-00089-A000) @ 60Hz, and from 200 to 250VAC (MT00-00090-A000) @ 50Hz. This is accomplished with the aid of a separate resonance winding across which an external 3.5Mfd capacitor is placed. **WARNING: This winding has an output voltage varying from 800 to 1000V peak-to-peak!**

This transformer reduces the line voltage to two center tap voltages: 8VAC and 15VAC, each having its own winding. This prevents high current draw on one voltage from influencing the other voltage.

A second transformer is used for isolation between the color monitor and line voltage. This line isolation also provides an AC voltage for the unregulated power supply and the auxiliary circuits, when implemented.

FILTER ASSEMBLY: The 8VAC and 15VAC from the Constant Voltage Transformer secondary windings are full-wave rectified by two power rectifiers each, MR-1120, and then filtered by a 100.000Mfd capacitor for the pre-regulated 8VDC and by a 55.000Mfd capacitor for the pre-regulated 15VDC. Both circuits are protected with a fuse: 10 Amp for the pre-regulated 8VDC and 6 Amp for the pre-regulated 15VDC. Both capacitors are discharged through a drainage resistor when the filter assembly is disconnected for any reason. Both center taps are connected together in this Filter Assembly to ensure that they are the same voltage level.

POWER CHASSIS: This is a combination of the transformers with the Filter Assemblies in order to comply with U.L., C.S.A., and V.D.E. safety regulations. It also incorporates the line filter, all line fuses, a safety switch, and the line power distribution. The Power Chassis will become available in the 3rd quarter of 1982.

+5V SOURCE: The pre-regulated 8VDC from the Filter Assembly is placed at the collector of the 2N3772 pass transistor and more or less of this voltage is allowed through depending on load and other factors. The actual regulator in this circuit is the LM305 which operates a 2N2905 amplifier. The LM305 senses the output voltage across the 160 ohm resistor, uses this wave form to control the base of the amplifier transistor, which is necessary in this circuit to provide enough current for the TIP 31 transistor, which in turn provides the current to operate the pass transistor. If the LM305 senses a drop in voltage, it turns on the amplifier transistor, which in turn activates the TIP 31 and the pass transistor. When the pass transistor is activated, it allows more voltage through to the output to compensate for the drop in voltage. The circuit also senses the amount of current through the 0.16 ohm resistor. If the current exceeds the safe limit determined by the value of the resistor, the amplifier is shut off which turns off the TIP 31 and thus the pass transistor. This limits the current to a safe level.

In order to minimize the power dissipation of the pass transistor, its pre-amplifiers and the LM305 are powered by the pre-regulated +15VDC. They are protected by a separate on-board 3/8 Amp fuse because in case of failure, the current draw would not be large enough to blow the 6 Amp fuse of the pre-regulated +15VDC. The 10 ohm/5W resistor is used to drop the voltage to prevent overheating of the pre-amplifiers and the LM305.

The SENSE LINE is used as the reference for the LM305 to compensate for any IR drop in the COM. LINE as discussed earlier. Adjustment provisions have been made by incorporating a voltage divider network with 2 resistors and a 100 ohm trim pot. By adjusting the trim pot, the LM305 can be further offset from the SENSE to compensate for any minor deviation. The resulting voltage is further filtered with a 470Mfd capacitor. The ferrite bead is used to prevent high frequency oscillation of the pass transistor, which would result in its self-destruction, usually by shorting the collector to the emitter. This would provide an unregulated 8VDC to the logic, destroying the logic chips.

+12V SOURCE: This power source operates in a similar manner as the +5V source, with a few minor differences. It has only one pre-amplifier, the current limiting resistor is 0.18 ohms, and no power dissipation minimizing technique is used, i.e. the LM305 and 2N2905 are powered by the same voltage as the pass transistor.

UNREGULATED SUPPLIES: The Power Supply PCB also generates an unregulated unfiltered auxiliary voltage which can be used to power indicator lights. This voltage is developed by full-wave bridge rectification of the voltage of the secondary winding of the line-isolation transformer. This semi-sinusoidal wave

form is then taken directly to the control circuitry of the indicator lights. Although this source is not used in some games, it is used in others where certain lights have to be controlled by the logic.

Furthermore, the above voltage is used to generate another voltage, the audio voltage. This audio voltage is developed by the same initial process used to create the unregulated unfiltered auxiliary voltage, however, it is further filtered by the 4700Mfd capacitor before this undulating voltage is sent to the Audio Amplifiers on the Game PCB.

NOTE: In some games the regulated +12V is used for audio.

ADDITIONAL FEATURES — (NOT USED IN ALL GAMES)

−5V SUPPLY: The 8V winding is again full-wave rectified, but since the cathodes of the two 1N4001 diodes are wired to the transformer secondary winding, this wave form is negative with respect to COM. This negative wave form is filtered by the 2000Mfd capacitor and placed at the input pin of the 7905 integrated voltage regulator. It can be further offset from −SENSE by adjusting the 100 ohm trim pot to compensate for any minor deviation from the specified −5V level. The resulting fully regulated voltage is further filtered by a 10Mfd capacitor to prevent load fluctuations from disturbing the operation of the regulator. The 7095 has internal overload protection.

RESET LINE: This part of the Power Supply PCB provides a power-on-clear signal when the game is first turned on — or — after a momentary power line failure. Since random information is loaded into many parts of the computer when power is first applied, this signal is necessary to clear this meaningless data away so the computer can start operating with a "clean slate". The reset circuit is divided into 5 distinct sections, each with its own function:

A. The OPTO-ISOLATOR provides voltage isolation from the line isolation transformer and is relatively insensitive to line voltage fluctuations and secondary voltage selection. The transformer output voltage can be varied from 9VAC to 14VAC. The output of the OPTO-ISOLATOR is a semi-square wave of 5V. (See AC Synch. on "Wave Shapes of Auxiliary Circuits" Figure 3.)

B. The PUMP CHARGER circuit detects if two or more AC cycles have dropped out (AC line failure). Its output will go to logic "1" approximately 40 milliseconds after the line voltage starts to drop out. When the line power is turned on initially, it acts as a power-on-reset circuit. Its output will rise with the +5V and stay at logic "1" at least until the +5VDC has stabilized, then it goes to logic "0". (See Pump Charge-out on "Wave Shapes of Auxiliary Circuits" Figure 3.) The output pulse is transferred to two circuits; the ONE-SHOT circuit and the LOGIC "OR" circuit.

C. The ONE-SHOT circuit is triggered by the positive edge of the pulse from the PUMP CHARGER and stretches it to at least 75 milliseconds. (See One-Shot-out on "Wave Shapes of Auxiliary Circuits" Figure 3.) This ensures that there will always be a proper reset pulse, regardless of the pulse length from the PUMP CHARGER circuit. (It does not respond when the power line is switched to "ON".) Its output pulse is transferred to the LOGIC "OR" circuit.

D. The LOGIC "OR" circuit operates just as its name implies. When it receives a logic "1" signal from either the PUMP CHARGER and/or the ONE-SHOT, it will pass it through to the AMPLIFIER.

E. The AMPLIFIER, consisting of the 2N4401 transistor, is used to provide sufficient current at logic "0". Its output is $\overline{\text{RESET}}$, which is used by the logic PCBs. (See $\overline{\text{RESET}}$ on "Wave Shapes of Auxiliary Circuits" Figure 3.)

F. A.C. SYNC for assemblies A082-90412-D000 / A082-90421-C000 and later versions. This 555 circuitry performs three functions at the same time:

1. It is a −2 frequency divider; the output of which is 50 or 60Hz, depending on the Line frequency.
2. It is a wave shaper. The output signal is squared and approximately 2ms long at Logic "0".
3. It is a current driver. It can sync or source 50ma and can directly interface with TTL.

BATTERY SUPPLY: This supply is used to provide current to a "Bookkeeping" RAM on the logic PCB when the line power fails or is turned off. Normally, with the line power "ON", +5VDC is supplied via the 0.22 microHenry inductor, the 82 ohm voltage dropping resistor, and a blocking diode. The voltage is regulated with a diode going to +5VDC. The Nickel-Cadmium rechargeable battery is charged via the 270 ohm charge current limiting resistor. When the line power is "OFF", the "Bookkeeping" RAM is supplied with a "stand-by" voltage of 3.6VDC to a 4.2VDC for a duration of at least 30 days.

No matter how advanced our technology becomes, it seems that a technician who understands power supplies can be successful at troubleshooting most electronic equipment. The reason for this is that many of the problems that occur are directly or indirectly related to the power supply.

At this time, we are going to look at the Bally Midway A082-90412/13 and A082-90421/22 type Power Supplies as seen in Omega Race, Kickman, and subsequent games. Since power supplies are generally not field serviceable, we are going to concentrate on diagnosis of a bad power supply. First, we have to know what the power supply's function is. Bally Midway's power supply is made up of several smaller supplies. They are: +5 volts regulated, +12 volts regulated, and unregulated audio and lamp voltages, and possibly a battery supply and/or −5 volts regulated.

The only purpose of a power supply is to give the proper voltage(s) and to supply enough current at the proper voltage(s) to fulfill the requirements of the game. These power supplies have current limiting features on all regulated sub-supplies. If the current demand is larger than its capabilities, first the voltage will drop, then it will shut itself off until the excess load is removed. It is quite possible that a power supply may be diagnosed "BAD" when in reality there is a short somewhere on one of the Logic Boards or elsewhere in the system. Symptoms of a bad power supply can be anything from no picture to specific functions not present on the screen. The best thing to do when you suspect a bad power supply is to check all the voltages with your meter. **Keep in mind that just because all the power supply voltages are present, this does not mean that the supply is good.** A power supply voltage can contain certain fluctuations that only an oscilloscope can detect. In this case, substitution is a good check. Approximate measurements can be made on the Power Supply PCB but accurate measurements **MUST** be made on the Logic PCB between the filter and the load.

CAUTION MUST BE TAKEN WHEN MAKING THESE MEASUREMENTS! IT'S POSSIBLE TO DAMAGE LOGIC COMPONENTS BY SHORTING POWER SUPPLY COMPONENTS!

+5 VOLTS REGULATED: This is the highest current supply on the board. Most of the devices on the game boards use this supply. To check it, put your meter ground probe on point "A" and its positive probe on point "B". You should read 5.0 volts to 5.3 volts. This supply is adjustable with a potentiometer.

NEVER ADJUST THIS POT WITHOUT A METER CONNECTED AS ABOVE!!

+12 VOLTS REGULATED: This supply is used for peripheral circuits. To check it, put your meter ground probe on point "A" and its positive probe on point "C". You should read 12.0 volts to 12.3 volts. It too is adjustable with a potentiometer.

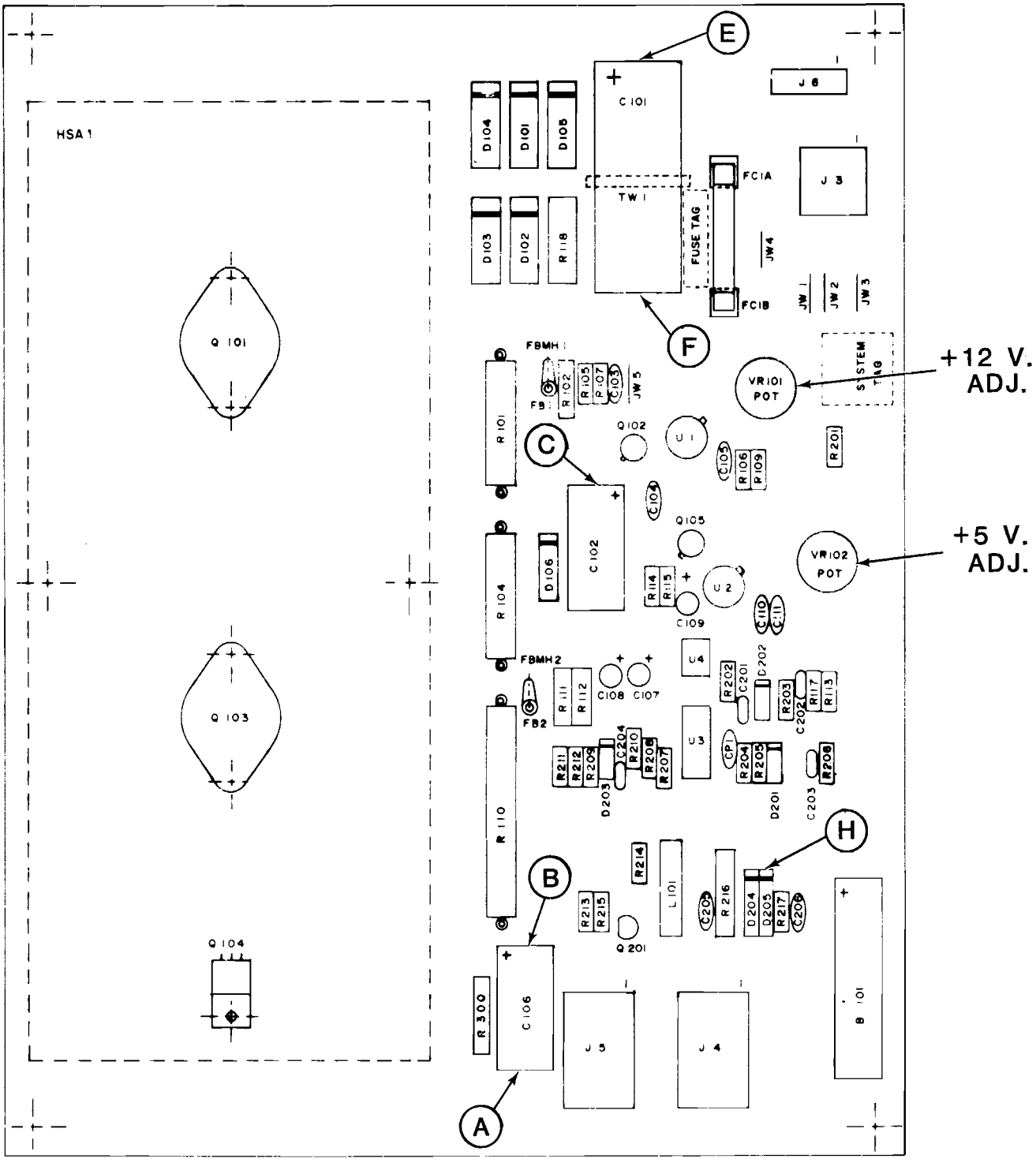
UNREGULAATED SUPPLIES: This is a supply used for audio and lamps. This supply can read from 9 volts to 16 volts. To check it, put your meter ground probe on point "E" and its positive probe on point "F".

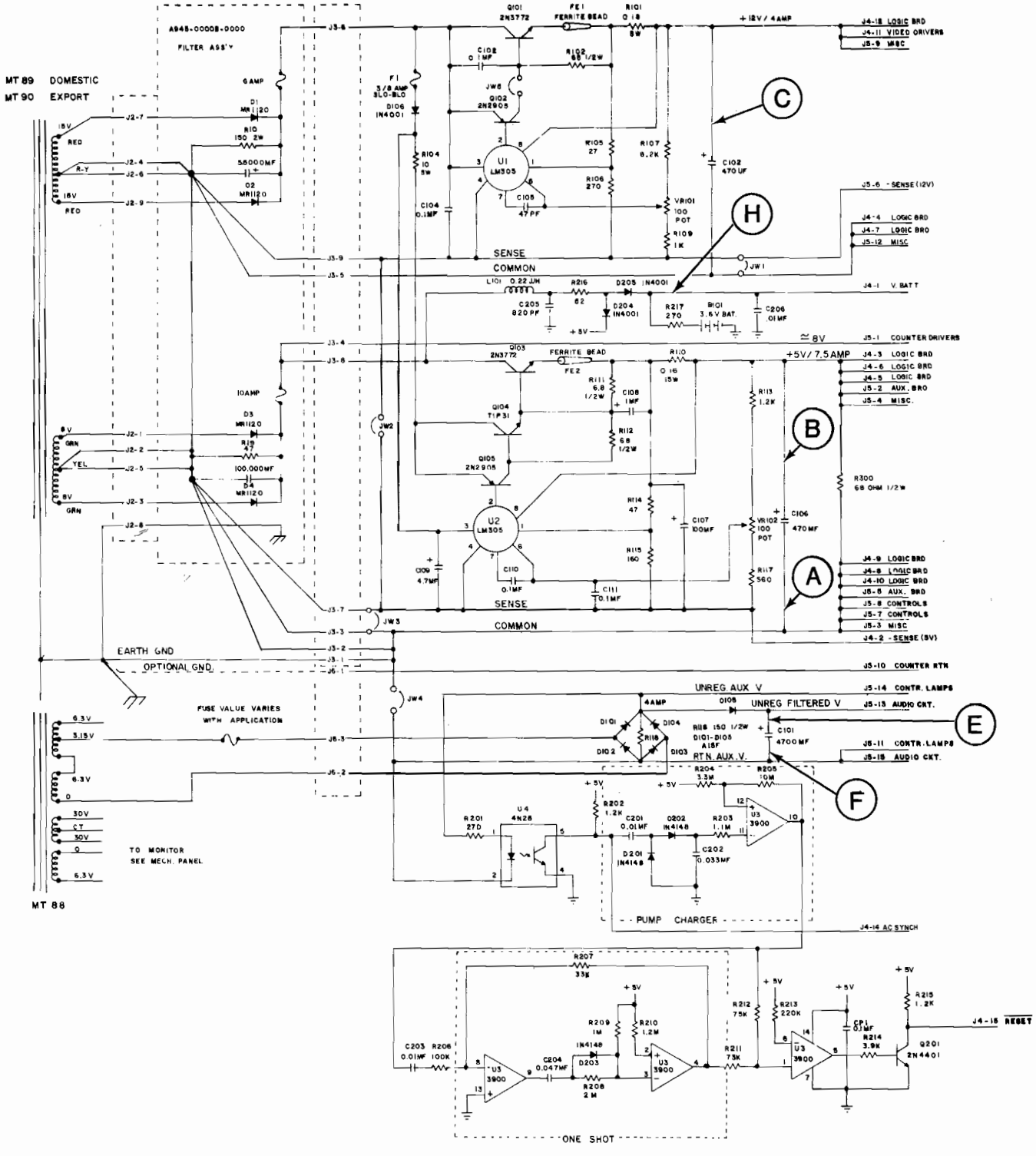
−5 VOLTS REGULATED: This supply is used by auxiliary circuitry and/or memories. To check it, put your meter ground probe on point "G" and its positive probe on point "A". You should read −4.9 volts to −5.2 volts. It too is adjustable with a potentiometer.

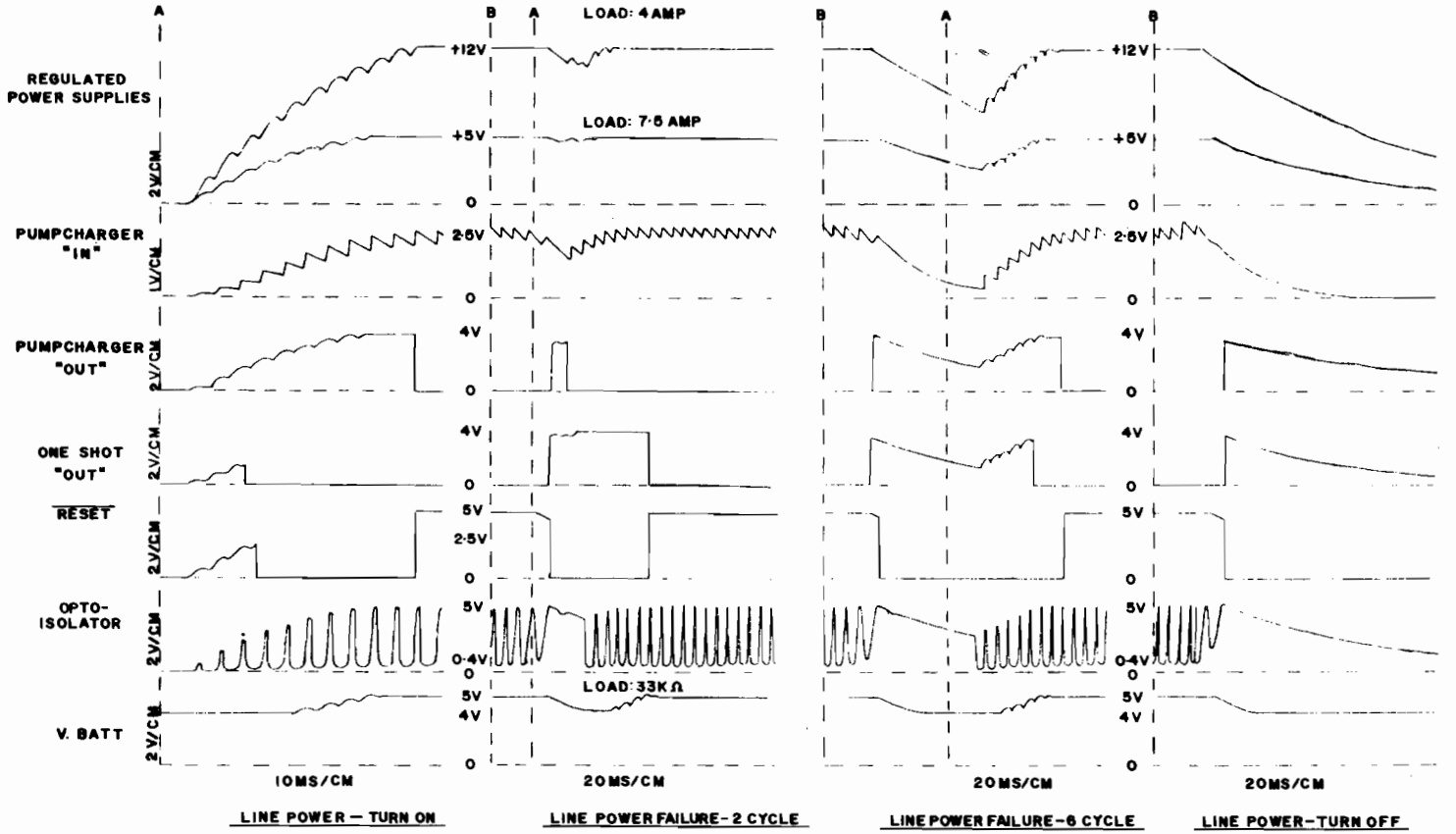
BATTERY SUPPLY: This supply is used by the "Bookkeeping" RAM. To check it, put your meter ground probe on point "[illegible]nd its positive probe on point "H". When the line power is "ON", you should read 5.0 to 5.3 volts. When the line power is "OFF", you should read 3.6 volts to 4.2 volts.

If all the voltage checks read good, there still is the chance your power supply is bad. With an oscilloscope, it can be determined whether a supply has a ripple, oscillation, or other type of failure.

If one of the supplies reads lower than it should (for example, the +5 volt supply reads +3 volts), turn off the game and pull the connector off that goes to the logic board(s). Short the Power Supply's −SENSE output to COMMON, turn the power back on, and check the supply again. If the supply is good, there is probably a bad device on one of the logic boards that is shorting the supply.


HSA 1
Q 101
Q 103
Q 104
E
F
C
B
A
H
C101
TW 1
FUSE TAG
FC1A
FC1B
J 6
J 3
J 5
J 4
D104
D101
D105
D103
D102
R118
JW4
JW1
JW2
JW3
FBMH1
FB1
R102
R105
P107
C103
JW5
R101
VR101 POT
+12 V. ADJ.
SYSTEM TAG
Q102
C105
R106
P109
R201
C104
C102
D106
Q105
R104
R114
R115
C109
C2
VR102 POT
+5 V. ADJ.
C110
C111
FBMH2
FB2
R111
R112
C108
C107
C4
C202
C201
C702
R203
R117
R113
C202
R211
R212
R209
C204
R210
R208
R207
C3
CP1
R204
R205
D203
D201
C203
R206
R110
R214
L101
R213
R215
Q201
C205
R216
D204
D205
R217
C206
R300
C106
B 101


MT 89 DOMESTIC
MT 90 EXPORT
MT 88
A948-00008-0000
FILTER ASS'Y
6 AMP
10 AMP
D1 MR1120
D2 MR1120
D3 MR1120
D4 MR1120
R10 150 2W
R19 47
58000MF
100,000MF
18V RED
R-Y
8V GRN
8V YEL
J2-7
J2-4
J2-6
J2-9
J2-1
J2-2
J2-5
J2-3
J2-8
EARTH GND
OPTIONAL GND.
FUSE VALUE VARIES WITH APPLICATION
6.3V
3.15V
6.3V
0
30V CT
30V
0
6.3V
TO MONITOR SEE MECH. PANEL
F1 3/8 AMP SLO-BLO
D106 IN4001
JW6
Q101 2N3772
FE1 FERRITE BEAD
R101 0.1Ω 8W
+12V / 4AMP
J4-18 LOGIC BRD
J4-11 VIDEO DRIVERS
J5-9 MISC
C102 0.1MF
R102 68 1/2W
Q102 2N2905
U1 LM305
R104 10 5W
R105 27
R106 270
R107 8.2K
C102 470 UF
C104 0.1MF
C108 47 PF
VR101 100 POT
R109 1K
J5-6 -SENSE (12V)
J4-4 LOGIC BRD
J4-7 LOGIC BRD
J5-12 MISC
SENSE
COMMON
JW1
J3-9
J3-5
L101 0.22 UH
R216 82
D205 IN4001
D204 IN4001
C205 820 PF
R217 270
B101 3.6 V BAT.
C206 01 MF
J4-1 V. BATT
+5V
≃8V
J5-1 COUNTER DRIVERS
J3-4
J3-6
Q103 2N3772
FERRITE BEAD FE2
R110 0.1Ω 15W
+5V/ 7.5 AMP
J4-3 LOGIC BRD
J4-6 LOGIC BRD
J4-5 LOGIC BRD
J5-2 AUX. BRD
J5-4 MISC.
R111 6.8 1/2W
C108 1MF
R113 1.2K
Q104 TIP31
R112 68 1/2W
Q105 2N2905
JW2
R300 68 OHM 1/2W
U2 LM305
R114 47
C107 100MF
VR102 100 POT
C106 470MF
R115 160
R117 560
C109 4.7MF
C110 0.1MF
C111 0.1MF
J4-9 LOGIC BRD
J4-8 LOGIC BRD
J4-10 LOGIC BRD
J5-6 AUX. BRD
J5-8 CONTROLS
J5-7 CONTROLS
J5-3 MISC
J4-2 -SENSE (5V)
SENSE
COMMON
JW3
J3-7
J3-3
J3-2
J3-1
J6-1
J5-10 COUNTER RTN
JW4
UNREG AUX. V
J5-14 CONTR. LAMPS
4AMP
D108
UNREG FILTERED V
J5-13 AUDIO CKT.
D101
D104
D102
D103
R118 150 1/2W
D101-D105 A15F
C101 4700 MF
RTN. AUX. V.
J5-11 CONTR. LAMPS
J5-15 AUDIO CKT.
J6-3
J6-2
R204 3.3M
R205 10M
+5V
R202 1.2K
U4 4N28
R201 270
C201 0.01MF
D202 IN4148
R203 1.1M
U3 3900
D201 IN4148
C202 0.033MF
PUMP CHARGER
J4-16 AC SYNCH
R207 33K
R209 1M
R210 1.2M
IN4148
C203 R208 0.01MF 100K
C204 0.047MF
D203
R208 2M
U3 3900
R212 75K
R213 220K
R211 75K
C211 .01MF
R214 3.9K
Q201 2N4401
R215 1.2K
J4-15 RESET
ONE SHOT
A
B
C
E
F
H



A = ACTUAL TURN-ON POINT OF LINE POWER
B = ACTUAL TURN-OFF POINT OF LINE POWER
TIME DELAY IS DUE TO TRANSFORMER REACTANCE.
USE 10MΩ OSCILLOSCOPE PROBES.

AUXILIARY CIRCUITS OF A082-90412-D000 AND A082-90421-C000

GAME VOLUME ADJUSTMENT CONTROL. (See Figure 1)

The game volume control pot is located just inside the cabinet on the right side of the coin door frame. There is only one pot. For adjustment, it may be reached through the coin door on **ALL** models.

To make the sounds louder, turn the pot clockwise as you face it ( ).

To make the sounds **less** loud, turn the pot counter-clockwise as you face it ( ).

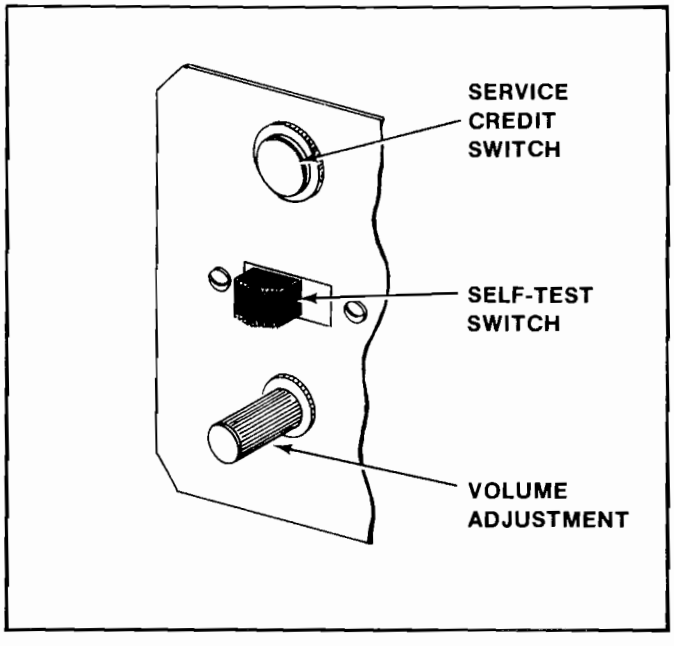


Figure 1 Game Volume Adjustment Control

OPTION SETTINGS:

To change the most common option settings, you **DO NOT** have to take the game apart or go into the cabinet and hunt for tiny switches on P.C. boards. These most common options can be changed from the main console of the game while it is in the Self-Test mode. The Self-Test switch is located just inside the cabinet on the right side of the coin door frame as you face it.

When changing any options, ALWAYS perform the Self-Test and play the game to be sure the ones selected are working properly. Of course, when you must change one of the switches that is located on one of the game's P.C. boards, it is also recommended that you perform the Self-Test and play the game to be sure the switches have worked properly and that no switches were accidentally moved that were not meant to be. (These switches are small and this can happen.)

The P.C. Board option switch settings, and what they will make the game do are shown in Figure **3.** These switches are MAINLY INTENDED for use by a technician who is checking and/or performing tests on the game. See Figure **2** for option switch locations.

NOTE: In order to set the option switches located on the game's P.C. Boards, these Boards need not be removed from their card rack.

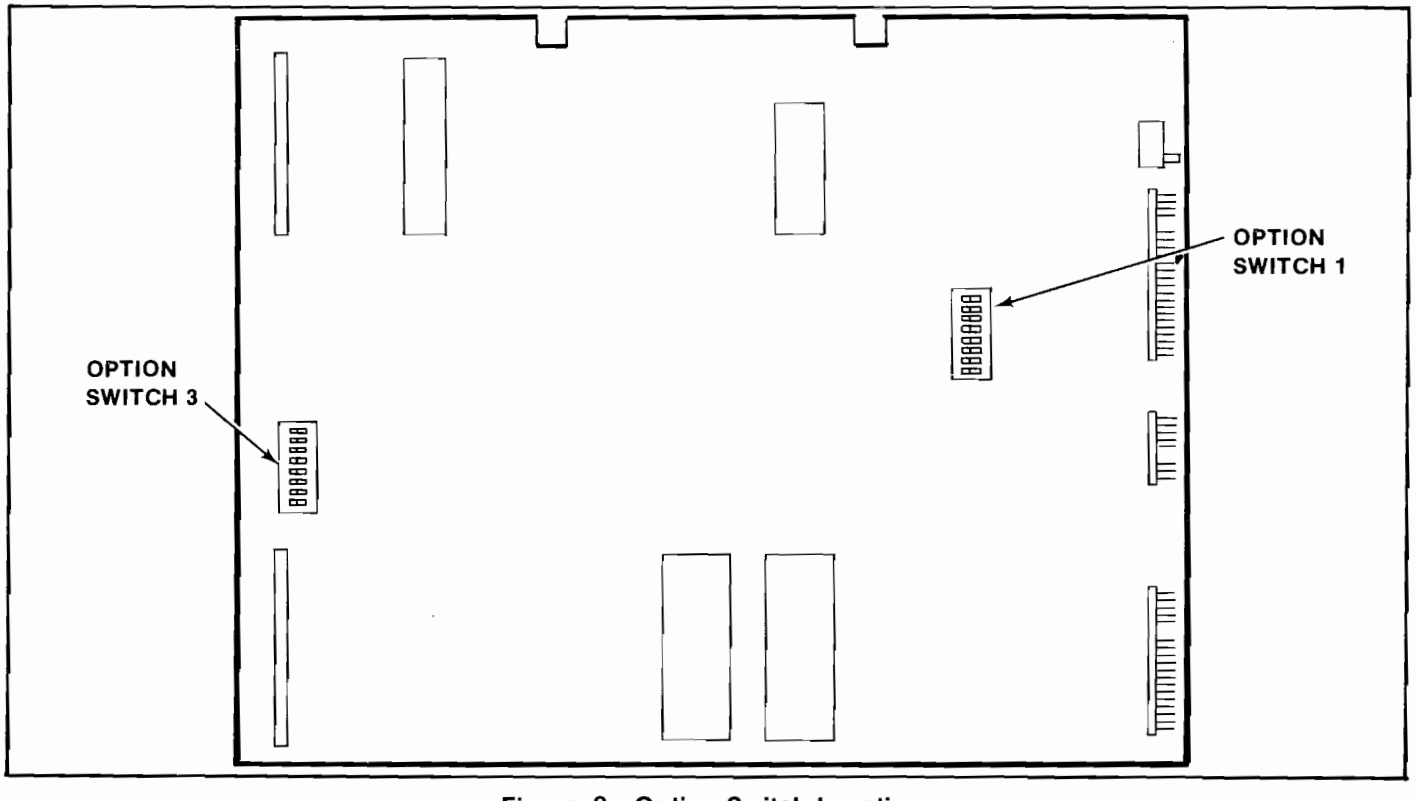


Figure 2 Option Switch Location

OPTION SWITCH SETTINGS

SWITCH NO. 1 — AT B 3 — LOCATED ON SOUND I/O P.C. BOARD

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8	SW#9	SW#10
2 COIN METERS	**ON**	NOT	NOT	NOT	NOT	NOT	NOT			
1 COIN METER	**OFF**	USED	USED	USED	USED	USED	USED			
MINI/UPRIGHT		**ON**								
COCKTAIL TABLE		**OFF**								
BUY IN ALLOWED			**ON**							
NO BUY IN			**OFF**							
FREEZE VIDEO										**ON**
NORMAL OPERATION										**OFF**

SWITCH NO. 3 — AT D 14 — LOCATED ON SOUND I/O P.C. BOARD

	SW#1	**SW#2	**SW#3	**SW#4
NORMAL OPERATION SOUND I/O DIAGNOSTIC MODE	**OFF** **ON**			
NORMAL OPERATION RAM/ROM TEST INDICATES TEST RESULTS VIA YELLOW LED ON SOUND I/O BOARD: **FAST FLASH** = **BAD ROM** **SLOW FLASH** = **BAD RAM**		**OFF** **ON**	THE REMAINDER OF MOST COMMON OPTION SETTINGS ARE CONDUCTED DURING THE **MACHINE SETUP** PORTION OF THE SELF-TEST MODE AND WILL BE COVERED IN DETAIL IN THAT SECTION OF THIS MANUAL	
NORMAL OPERATION OSCILLATOR TEST			**OFF** **ON**	
NORMAL OPERATION FILTER TEST				**OFF** **ON**

NO EFFECT IF **SW#1 OF SWITCH NO. 3 IS IN THE "**OFF**" POSITION.

Figure 3 Option Switch Settings

SELF-TEST MODE

The Self-Test mode is a special mode for checking game play statistics as well as game switches and computer functions. It is the easiest and best way to check for proper operation of the entire game.

NOTE: Putting the game into Self-Test **WILL NOT** cause the game to erase any CREDITS it has in its memory when the Self-Test mode is entered.

You may begin a Self-Test at any time by sliding the Self-Test switch to the "ON" position after the power to the game is on (the Self-Test switch is located just inside the cabinet on the right side of the coin door frame as you face it). When this is done, the game will react as follows:

1. If the game is in the Attract mode when the Self-Test switch is moved to the "ON" position, it will finish the sequence and then go into the Self-Test mode. This is illustrated by the display of the Self-Test Mode Menue on the monitor screen.
2. If the game is in the Ready-To-Play mode or the Play mode when the Self-Test switch is slid to the "ON" position, it **WILL NOT** go into the Self-Test mode until **AFTER** the players' last TRON has been eliminated (the game MUST be over). At this point, the game will go into the Self-Test mode. Again, this is illustrated by the display of the Self-Test Mode Menue on the monitor screen.
3. The fastest way to enter the Self-Test mode is to slide the Self-Test switch to the "ON" position and then activate the "TILT" switch located on the back side of the coin door just below the lock mechanism. The game will then **IMMEDIATELY** go into the Self-Test mode.

The Self-Test mode has eight (8) major categories as illustrated by Figure **4.**

1. It is easy to select what category you want to enter. By pushing forward or pulling backward on the controler stick, the Cursor at the left of the screen can be moved UP and DOWN, (forward=UP) and (backward=DOWN), until it is in front of the category you want to test. Release the controler stick at this time.
2. After the Cursor has been positioned, pull the trigger on the controler stick and the monitor screen will display the test category you have selected.

NOTE: There is one exception to this. If you position the Cursor in front of the "PRESET" category on the Self-Test Mode Menue, when you pull the trigger on the controler stick — EVERYTHING, I repeat — **EVERYTHING;** including **ALL** information in the "BOOKKEEPING" mode, and **ALL operator selected options,** will be set back to zero "0" and to the factory recommended settings — **respectively.**

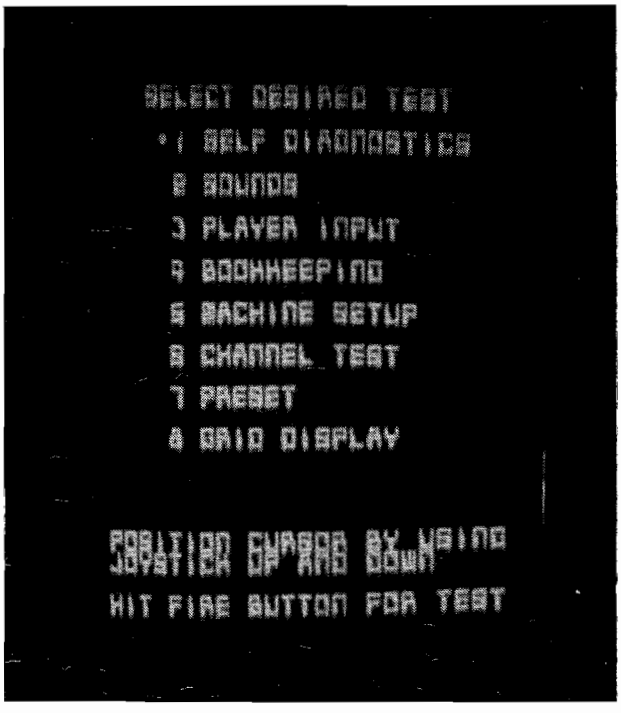


Figure 4 Self-Test—Menu

- ☐ Once you are **IN** one of the Self-Test mode categories, FOLLOW THE **ON-SCREEN** INSTRUCTIONS TO **COMPLETE** THE TEST.

3. The next group of figures shows the **CORRECT** screen presentation for **EACH** category of the Self-Test mode.

During the SELF DIAGNOSTICS section of the Self-Test mode, you will **first** see a cross hatch pattern on the screen for about 1/2 second. **Second,** you will see a lot of different colored bars shown on the monitor screen. These bars will be UNpainted one at a time from the top down. **Third,** you will see the screen painted Red, Blue, and Green in bars from the top down. **Fourth,** another group of colored bars is displayed. This sequence is repeated several times. And finally, this sequence is replaced by this message: **"HIT FIRE BUTTON TO EXIT".** If the Fire button is not hit, the test will repeat itself. This feature was designed into the game to enable over-night testing for an intermittent hardware problem.

If the SELF DIAGNOSTICS find one or more bad ROM or RAM chips: instead of going through what is described above, the game will give you a written message as to which parts are bad. This message includes their I.D.'s and their P.C. Board locations.

During the SOUNDS sections of the Self-Test mode, the game will give a display which looks like that shown in Figure **5.**

- ☐ In this category, each of the game's 24 separate sounds can be checked individually in any order — or — you can tell the game to check them all in order — 3 through 26.

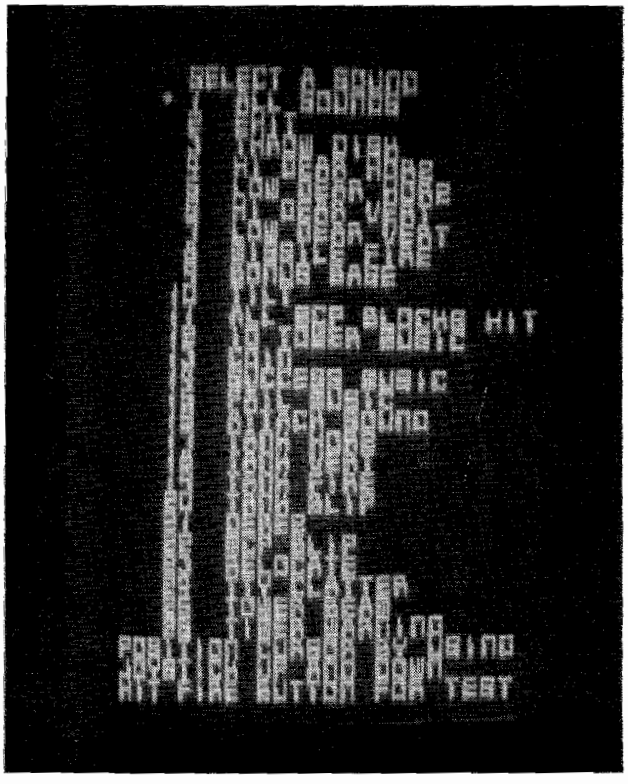
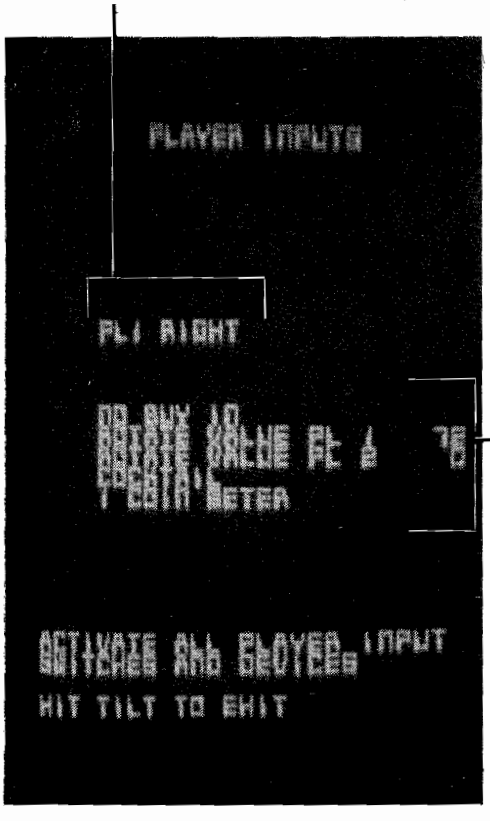


Figure 5 Self-Test—Sounds

As the Player Input Switches and Devices are activated, the Switch or Device activated is spelled out in the space indicated.



This is a P.C.B. switch setting.

Figure 6 Self-Test—Player Input

During the PLAYER INPUT section of the Self-Test mode, the game will give a display which looks like that shown in Figure 6.

- In this category, each of the game's player operated controls — including the coin switches on the back side of the coin door — may be check individually. A game sound will be heard as each switch/control is actuated. If no game sound is heard, that switch/control is either not working, miswired, or disconnected. Check it out thoroughly.

During the BOOKKEEPING section of the Self-Test mode, the game will give a display which looks like that shown in Figure 7.

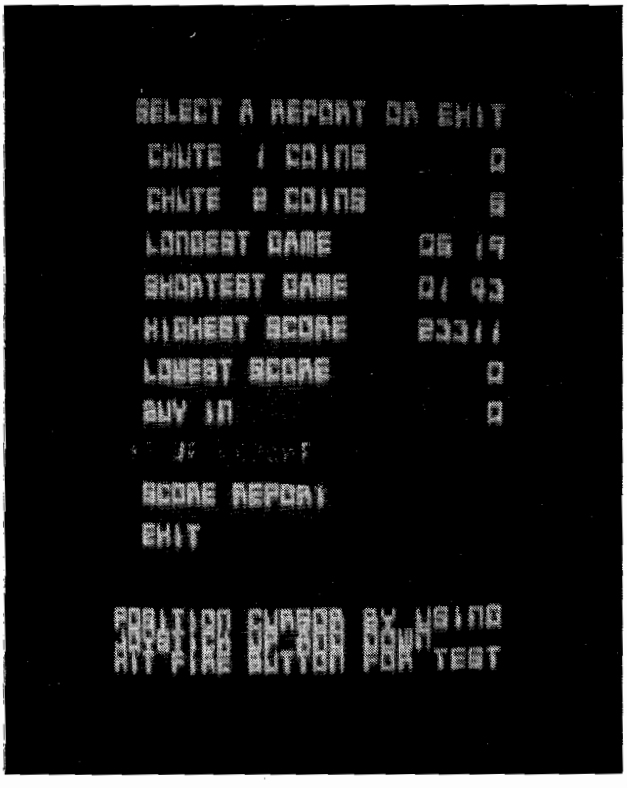


Figure 7 Self-Test—Bookkeeping

- In this category a basic bookkeeping function is performed. And with the selection of the "TIME REPORT" and the "SCORE REPORT", detailed breakdowns of game times and scores may be obtained.

In the TIME REPORT and SCORE REPORT sections of the BOOKKEEPING mode, the game will give displays which look like those shown in Figures 8 and 9 respectively.

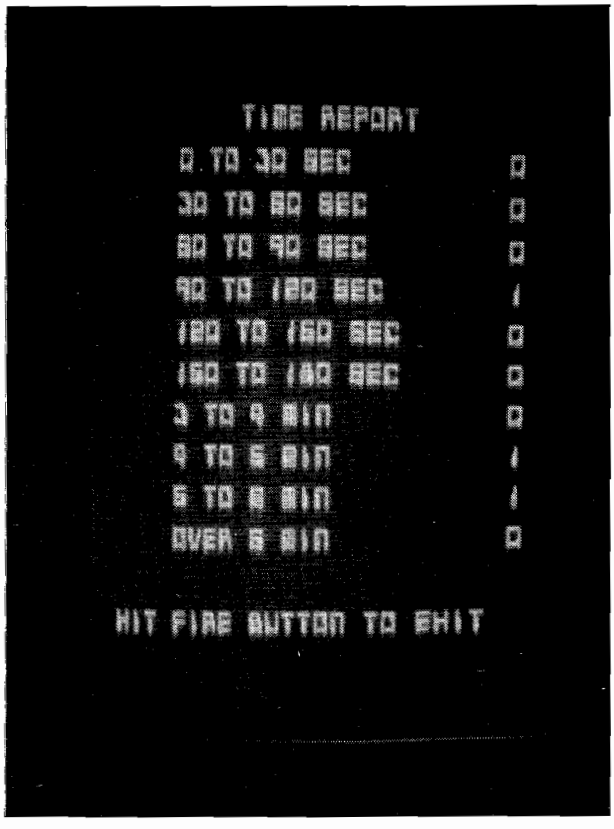


Figure 8 Self-Test—Time Report

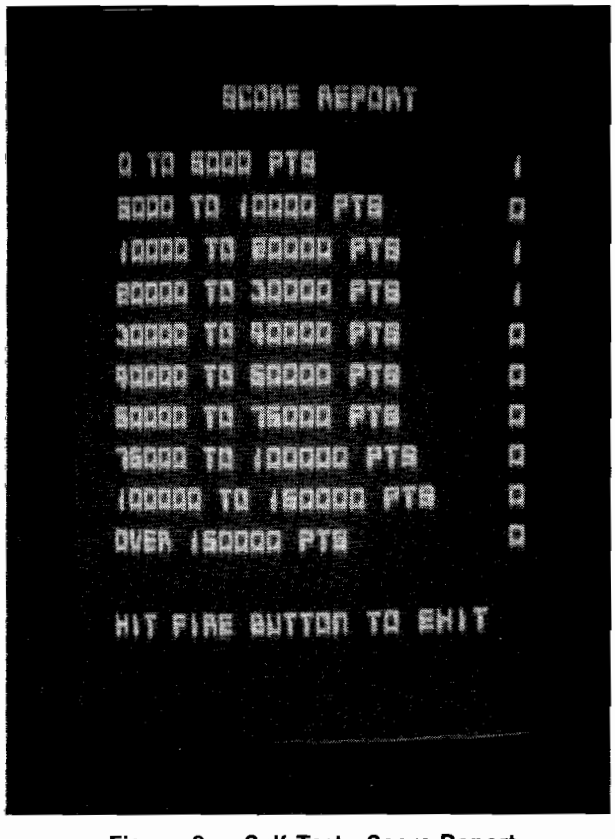
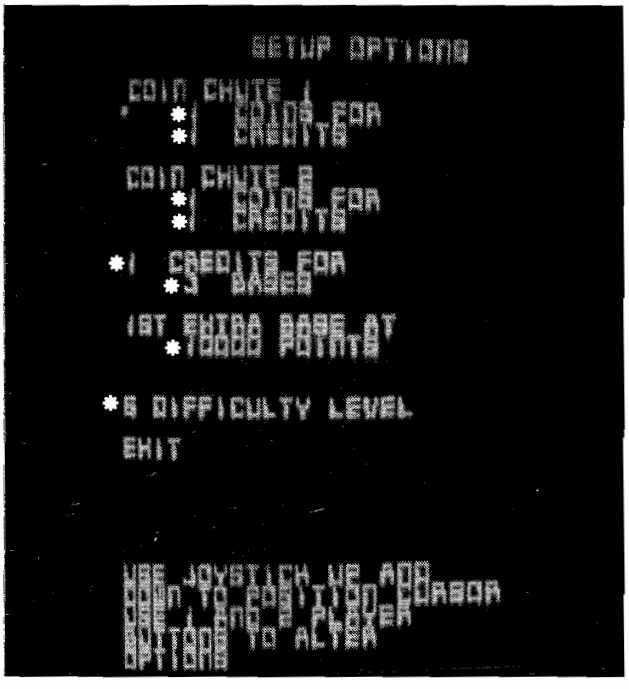


Figure 9 Self-Test—Score Report

During the SETUP OPTIONS section of the Self-Test mode, the game will give a display which looks like that shown in Figure **10.**



*** = Factory recommended settings.**

Figure 10 Self-Test—Setup Options

- In this category, all common game options may be changed from the control console: coins per credit, credits per base, bonus base(s) awarded at, difficulty level --, and so on.

The Difficulty Level setting has a range of 1 to 9 with 1 representing the easiest level of play and 9 representing the most difficult level of play. One is the factory recommended setting.

During the CHANNEL TEST section of the Self-Test mode, the game will give a display which looks like that shown in Figure **11.**

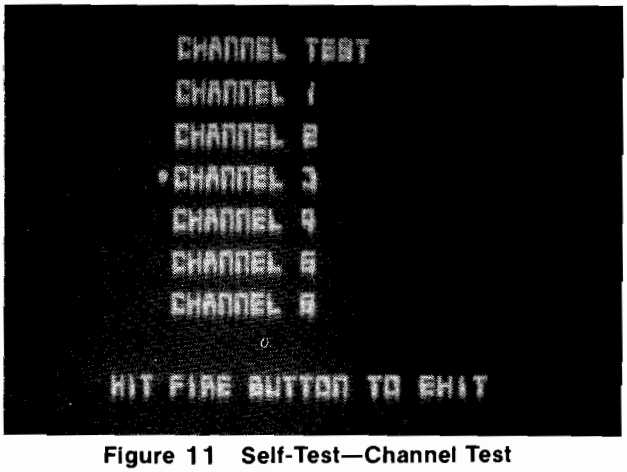


Figure 11 Self-Test—Channel Test

- In this category, the game conducts a test of its SOUND SYSTEM.

A Glossary of Microprocessor Terms

MICROPROCESSOR — one or several microcircuits that perform the function of a computer's CPU. Sections of the circuit have arithmetic and comparative functions that perform computations and executive instructions.

CPU — central-processing unit. A computing system's "brain", whose arithmetic, control and logic elements direct functions and perform computations. The microprocessor section of a microcomputer is on one chip or several chips.

PROM — programmable read-only memory. User permanently sets binary on-off bits in each cell by selectively fusing or not fusing electrical links. Nonerasable. Used for low-volume applications.

EPROM — erasable, programmable, read-only memory. Can be erased by ultraviolet light bath, then reprogrammed. Frequently used during design and development to get programs debugged, then replaced by ROM for mass production.

ROM — read-only memory. The program, or binary on-off bit pattern, is set into ROM during manufacture, usually as part of the last metal layer put onto the chip. Nonerasable. Typical ROM's contain up to 16,000 bits of data to serve as the microprocessor's basic instructions.

RAM — random-access memory. Stores binary bits as electrical charges in transistor memory cells. Can be read or modified through the CPU. Stores input instructions and results. Erased when power is turned off.

LSI — large scale integration. Formation of hundreds or thousands of so-called gate circuits on semiconductor chips. Very large scale integration (VLS) involves microcircuits with the greatest component density.

MOS — metal-oxide semiconductor. A layered construction technique for integrated circuits that achieves high component densities. Variations in MOS chip structures create circuits with speed and low-power requirements, or other advantages (static will damage a MOS chip).

Introduction to the Z-80 CPU

The term "microcomputer" has been used to describe virtually every type of small computing device designed within the last few years. This term has been applied to everything from simple "microprogrammed" controllers constructed out of TTL MSI up to low end minicomputers with a portion of the CPU constructed out of TTL LSI "bit slices." However, the major impact of the LSI technology within the last few years has been with MOS LSI. With this technology, it is possible to fabricate complete and very powerful computer systems with only a few MOS LSI components.

The Zilog Z-80 family of components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices a computer can be constructed with capabilities that only a minicomputer could previously deliver.

New products using the MOS LSI microcomputer are being developed at an extraordinary rate. The Zilog Z-80 component set has been designed to fit into this market through the following factors:

1. The Z-80 is fully software compatible with the popular 8080A CPU.
2. Existing designs can be easily converted to include the Z-80.
3. The Z-80 component set is at present superior in both software and hardware capabilities to any other microcomputer system on the market today.
4. For increased throughput the Z80A operating at a 4 MHZ clock rate offers the user significant speed advantages.

Microcomputer systems are extremely simple to construct using Z-80 components. Any such system consists of three parts:

1. **CPU (Central Processing Unit)**
2. **Memory**
3. **Interface Circuits to peripheral devices**

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and in most cases data that is to be processed. For example, a typical instruction sequence may be to read data from a specific peripheral device, store it in a location in memory, check the parity and write it out to another peripheral device. Note that the Zilog component set includes the CPU and various general purpose I/O device controllers, while a wide range of memory devices may be used from any source. Thus, all required components can be connected together in a very simple manner with virtually no other external logic.

General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange command need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

Arithmetic & Logic Unit (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

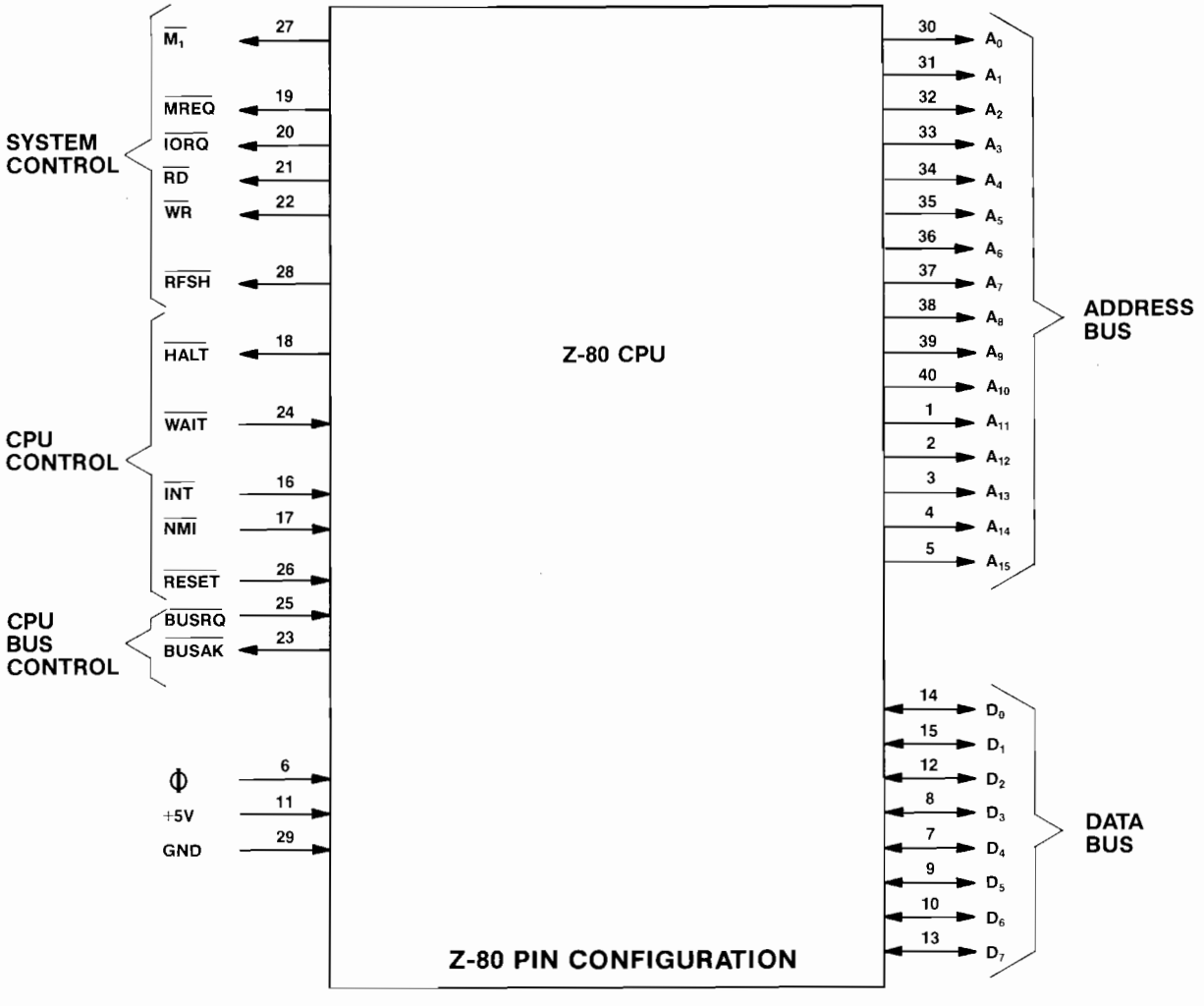
Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set bit
Logical Exlusive OR	Reset bit
Compare	Test bit

Instruction Register and CPU Control

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

Z-80 CPU Pin Description

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in the below figure and the function of each is described.



A_0-A_{15}
(Address Bus)
Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7
(Data Bus)
Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

M_1
(Machine Cycle one)
Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M1}$ is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. $\overline{M1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

MREQ
(Memory Request)
Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

IORQ
(Input/Output Request)
Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.

RD
(Memory Read)
Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

WR
(Memory Write)
Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

RFSH
(Refresh)
Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.

HALT
(Halt state)
Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

WAIT
(Wait)
Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

INT
(Interrupt Request)
Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).

NMI
(Non-Maskable Interrupt)
Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous $\overline{WAIT}$ cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override a $\overline{NMI}$.

RESET
Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

1) Disable the interrupt enable flip-flop

2) Set Register I = 00H

3) Set Register R =00H

4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control ouput signals go to the inactive state.

BUSRQ
(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.

BUSAK
(Bus Acknowledge)

Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

CLK
(Clock)

Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

MCR II SYSTEM
P.C. BOARD JUMPER OPTIONS

VIDEO GENERATOR P.C. BOARD

MANUFACTURER	EPROM NO.	JW#1	JW#2	JW#3	JW#4	JW#5	JW#6	JW#7	JW#8
MOTOROLA	68764	#	*	*	#	*	*	*	*
	68766	#	*	*	#	*	*	*	*
INTEL	2764	*	#	#	*	#	*	*	#
T. I.	2564	#	*	*	#	*	#	#	*

SUPER C.P.U. P.C. BOARD

JUMPER OPTIONS FOR PROGRAM ROMS ONLY

MANUFACTURER	EPROM NO.	JW#2	JW#4	JW#5	JW#6	JW#7	JW#18	JW#19	
MOTOROLA	68764	#	#	*	#	*	*	#	
	68766	#	#	*	#	*	*	#	
T. I.	2564	#	#	*	#	*	*	#	
INTEL	2764	*	*	#	*	#	#	*	

JUMPER OPTIONS FOR BACKGROUND ROMS ONLY

MANUFACTURER	EPROM NO.	JW#10	JW#11	JW#12	JW#13	JW#14	JW#15	JW#16	JW#17
MOTOROLA	68764	*	#	*	#	*	#	#	*
	68766	*	#	*	#	*	#	#	*
T. I.	2564	*	#	*	#	*	#	#	*
INTEL	2764	#	*	#	*	#	*	*	#

SOUND I/O P. C. BOARD

MANUFACTURER	EPROM NO.	JW#1	JW#2
NUMEROUS MFR'S	2532	*	#
NUMEROUS MFR'S	2732	#	*

* = CUT JUMPER WIRES WHERE THIS SYMBOL "*" APPEARS.
# = LEAVE JUMPER WIRES IN WHERE THIS SYMBOL "#" APPEARS.

The above table illustrates the fact that the Video Generator P.C. Board used in the MCR II System has 8 jumper wires, the SUPER C.P.U. P.C. Board used in the MCR II System has 19 jumper wires, and the Sound I/O P.C. Board used in the MCR II System has 2 jumper wires.

All of the above Boards can be used with a variety of different **SETS of EPROM chips.** However, these EPROMS are not all made by the same manufacturer and do have some internal differences. So, in order to make them function properly in their respective P.C. Boards, certain jumper wires on these Boards have to be cut.

The above table tells you which jumpers to cut (depending on which EPROM set you're going to use) by showing a "*" under that jumper wire's number. If there is **NO "*"** under a jumper wire's number, THAT PARTICULAR JUMPER WIRE **IS NOT TO BE CUT.**

REVISIONS

MIDWAY MFG. CO.
FRANKLIN PK. ILL.

PART NO. M051-00986-E011

A082-90910-E000, DUAL POWER AMP, SCHEMATIC

SCALE NONE

NO. REQ'D PER.

USED ON TRON

HEAT TREAT

MAT'L.

FINISH

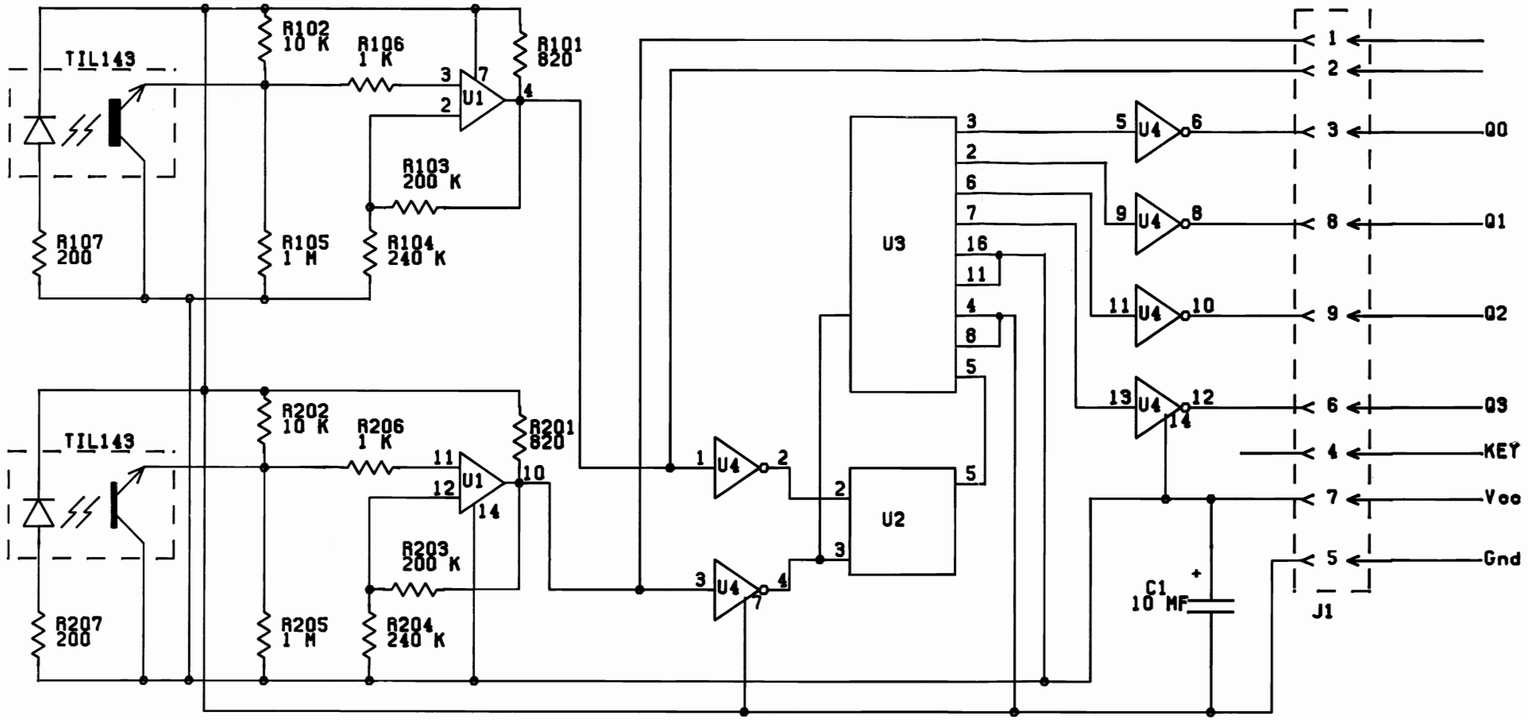
DRN

CKD

DATE 5/17/82

DO NOT SCALE DWG.

DIM. TOLERANCES UNLESS SPECIFIED
CONCENTRICITY T I R .003
FRACTIONAL ± 1/64
DECIMAL ± .005
HOLE DIA. + .002 .000



NOTES

U1-LM3900
U2-7474
U3-74191
U4-7414

PROJECT ENG: C.MEDNICK

CKD.	DO NOT SCALE DWG.		REVISIONS
DRN. TJK	DATE 8/26/81	USED ON	MIDWAY MFG. CO. FRANKLIN PK. ILL.
heat treat	scale FULL	NO. REQ'D 1 PER	
mat'l.	BINARY ANGLE DECODER SCHEMATIC A082-91391-C000		PART NO. M051-00968-C004
finish			

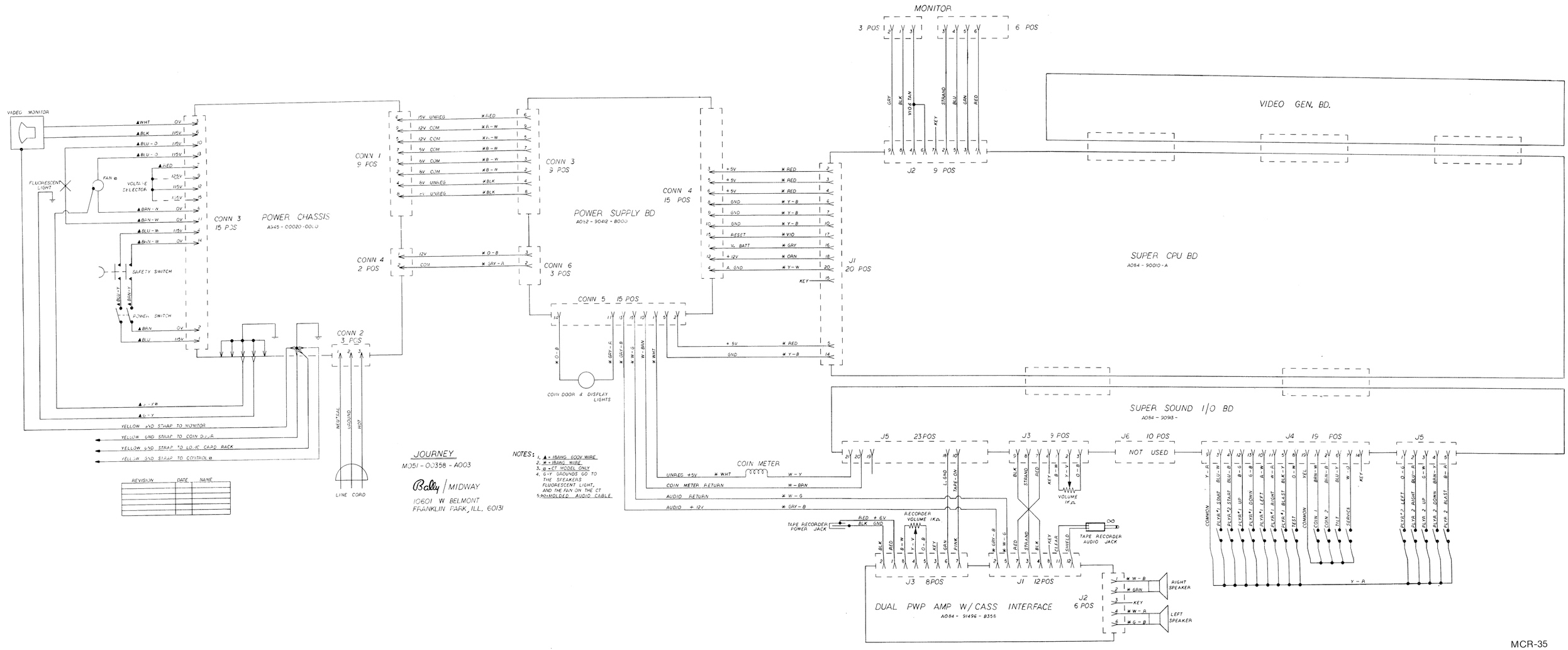
Chip Number	Function
MB8416	Ram 2K x 8
6116LP-4	Ram 2K x 8
9860-07AXN-AXHD	PROM 82S123 (SB2-A)
Z-80 CTC	Counter timer circuit
0066-313BX-XXQX (MMC01)	H-T generator - custom
0066-314BX-XXQX (MMC02)	V-T generator - custom
0066-315BX-XXQX (MMC03)	Misc. V & H circuits - custom
0066-316BX-XXQX (MMC06)	Misc. TTL circuits - custom
0066-322BX-XXQX (MMC04)	NVR controller - custom
AY-3-8910 (8910)	Sound generator
LM3900	Quad operational amplifier
MC3403	Quad operational amplifier

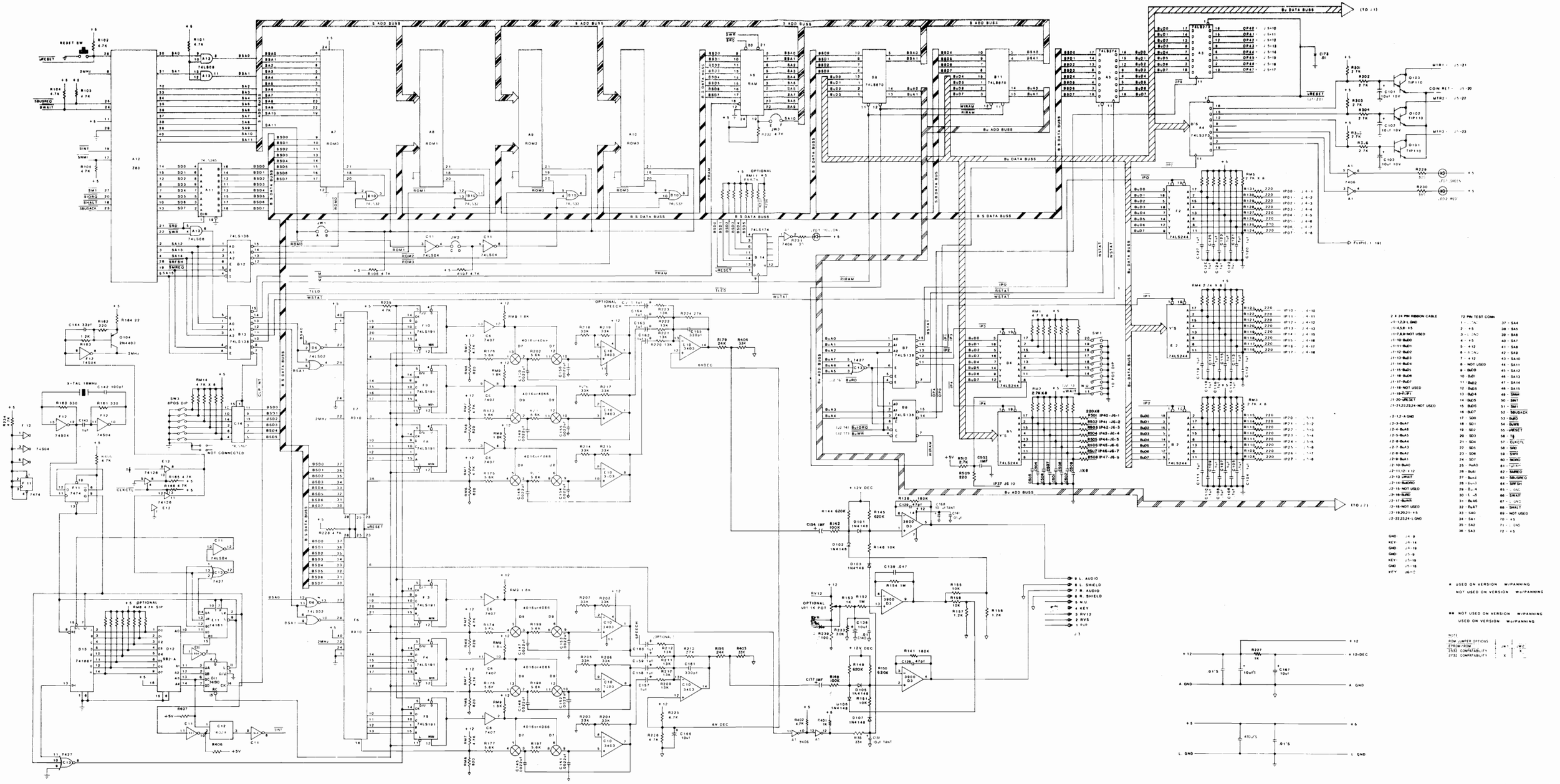
Misc. Components

16.00 & 19.9 MHZ	Z-TAL
2N4123	Transistor NPN
2N4403	Transistor PNP
MPSA70	Transistor PNP
TIP110	Transistor NPN

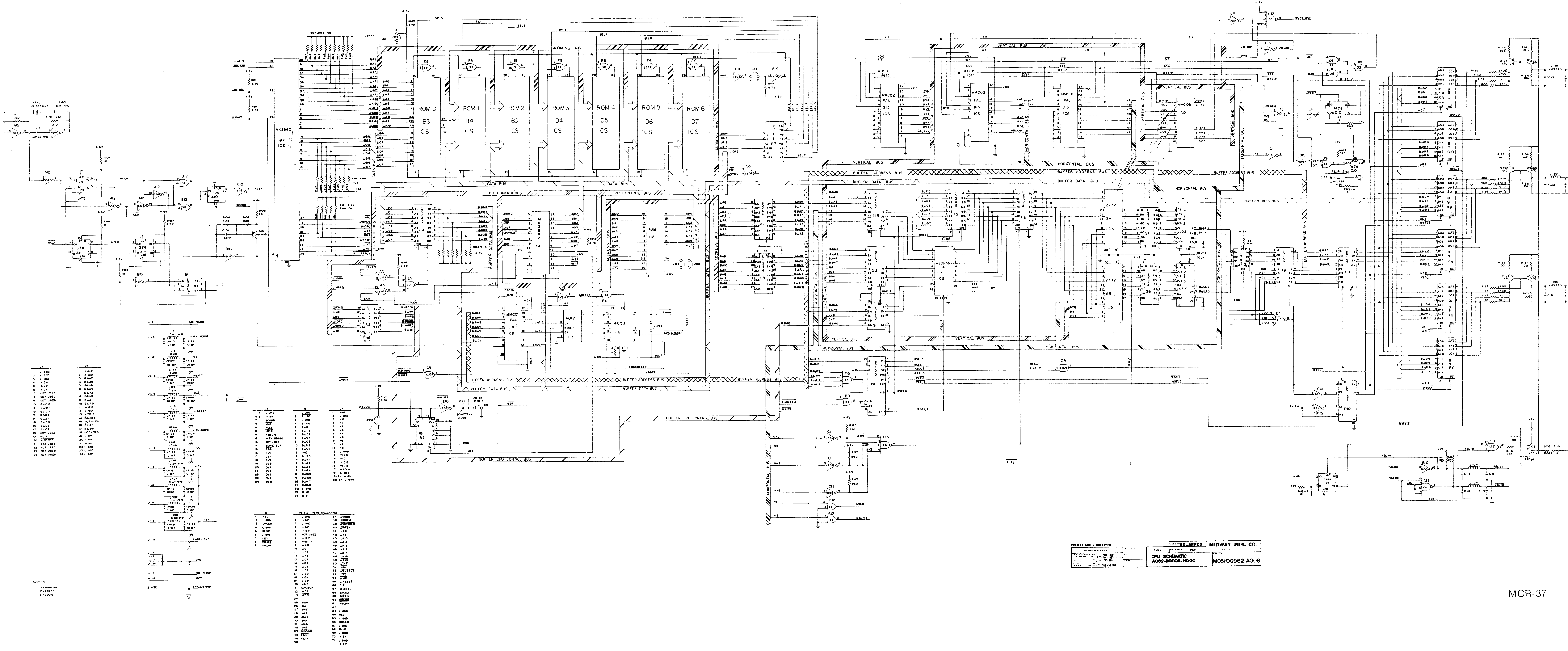
Logic Boards Integrated Circuits

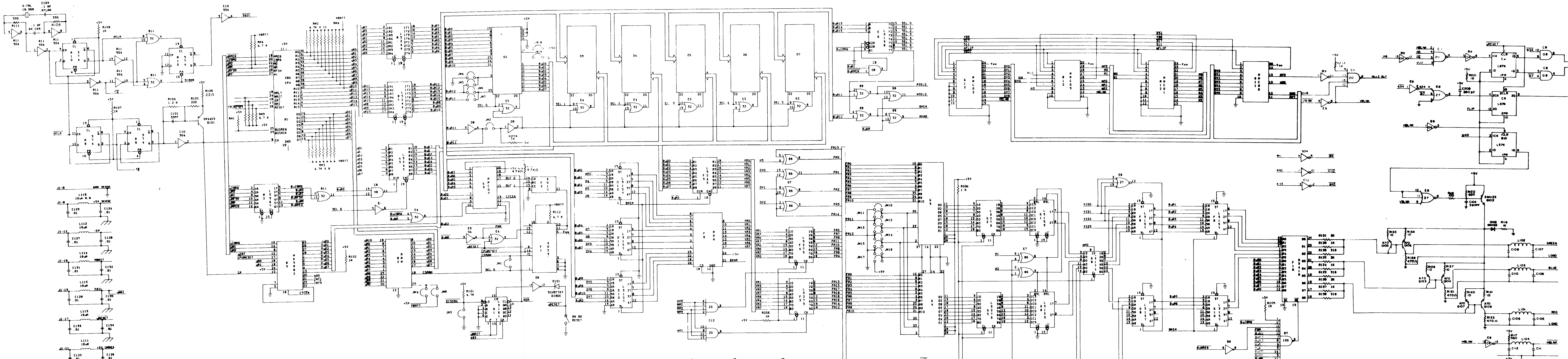
Chip Number	Function
7400	Quad 2 input Nand
74LS02	Quad 2 input Nor
74LS04	Hex inverter
7406	Hex inverter open collector
7407	Hex buffer open collector
74LS08	Quad 2 input And
74LS20	Dual 4 input Nand
7427	Triple 3 input Nor
74LS30	8 input Nand
74LS32	Quad 2 input Or
74LS74	Dual "D" Flip-Flop
74LS86	Quad 2 input exclusive Or
7489	64 bit ram 16 x 4
74126	Quad buffer tri-state
74LS138	3 to 8 line decoder
74LS153	Dual 4 to 1 line multiplexer
74LS155	Dual 2 to 4 line decoder
74LS157	Quad 2 to 1 line multiplexer
74160	4 bit decade counter
74161	4 bit binary counter
74166	8 bit shift register
74LS174	Hex "D" Flip-Flop
74175	Quad "D" Flip-Flop
74LS191	Up/down binary counter
74LS194	8 bit shift register
74LS244	Octal buffer tri-state
74LS245	Octal buss transceiver
74LS273	Octal "D" Flip-Flop
74LS283	4 bit full adder
74LS367	Hex buss driver
74LS374	Octal "D" Flip-Flop tri-state
74LS670	4 x 4 register files
4017	Decade counter/divider
14016	Quad analog switch
14024	7 stage ripple counter
14053	Triple 2 channel analog multiplexer
Z80	CPU 2.5 MHz
Z80A	CPU 4 MHz
D780C	CPU 2.5 MHz
D780C-1	CPU 4 MHz
TMS2564	8K x 8 EPROM
MBM2732	4K x 8 EPROM
HN462532	4K x 8 EPROM
2114	Ram 1K x 4
93422	Ram 256 x 4
M58725	Ram 2K x 8
4801AN-90	Ram 1K x 8
4118A-4	Ram 1K x 8
93419 or 82S09	64 X 9 Color Ram
74LS133	13 input Nand Gate

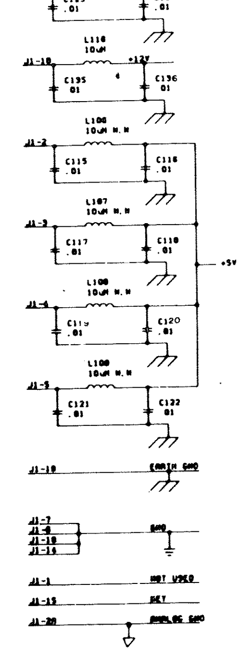

MONITOR
3 POS
6 POS
GRY
BLK
VIO
TAN
KEY
STRAND
BLU
GRN
RED
J2 9 POS
VIDEO GEN. BD.
VIDEO MONITOR
FLUORESCENT LIGHT
FAN
VOLTAGE SELECTOR
SAFETY SWITCH
POWER SWITCH
CONN 3
15 POS
POWER CHASSIS
A045 - 00020 - 0000
CONN 1
9 POS
CONN 4
2 POS
CONN 3
3 POS
CONN 6
3 POS
POWER SUPPLY BD
A052 - 90412 - B000
CONN 4
15 POS
J1
20 POS
SUPER CPU BD
A084 - 90010 - A
CONN 5 15 POS
COIN DOOR & DISPLAY LIGHTS
CONN 2
3 POS
NEUTRAL
GROUND
HOT
LINE CORD
YELLOW GND STRAP TO MONITOR
YELLOW GND STRAP TO COIN DOOR
YELLOW GND STRAP TO LOGIC CARD RACK
YELLOW GND STRAP TO CONTROLS
SUPER SOUND I/O BD
A084 - 90913 -
J5 23 POS
J3 9 POS
J6 10 POS
NOT USED
J4 19 POS
J5
COIN METER
UNREG +5V
COIN METER RETURN
AUDIO RETURN
AUDIO +12V
L GND
TAKE-ON
VOLUME 1K
TAPE RECORDER POWER JACK
RED +6V
BLK GND
RECORDER VOLUME 1KΩ
TAPE RECORDER AUDIO JACK
J3 8POS
J1 12POS
J2 6 POS
DUAL PWR AMP W/ CASS INTERFACE
A084 - 91496 - B356
RIGHT SPEAKER
LEFT SPEAKER
JOURNEY
M051 - 00358 - A003
Bally / MIDWAY
10601 W BELMONT
FRANKLIN PARK, ILL. 60131
NOTES:
1. ▲ = 18AWG BOOK WIRE
2. ✱ = 18AWG WIRE
3. ⊕ = CT MODEL ONLY
4. G-Y GROUNDS GO TO THE SPEAKERS FLUORESCENT LIGHT, AND THE FAN ON THE CT
5. 90✱✱MOLDED AUDIO CABLE
REVISION
DATE
NAME



DO NOT SCALE DWG	1 PER
6/23/82	SCHEMATIC DRAWING SUPER SOUND I/O A084-90913-E000
	MIDWAY MFG. CO. M051-00628-A014


MK3880
B7
ICS
ROM 0
B3
ICS
ROM 1
B4
ICS
ROM 2
B5
ICS
ROM 3
D4
ICS
ROM 4
D5
ICS
ROM 5
D6
ICS
ROM 6
D7
ICS
ADDRESS BUS
DATA BUS
CPU CONTROL BUS
RAM
D8
4017
F3
4053
F2
MMC01
PAL
E4
ICS
MMC02
PAL
G13
ICS
MMC03
PAL
B13
ICS
MMC01
PAL
A13
ICS
MMC06
G2
VERTICAL BUS
HORIZONTAL BUS
BUFFER ADDRESS BUS
BUFFER DATA BUS
BUFFER CPU CONTROL BUS
2732
C5
2732
G5
4801AN
F7
ICS
PROJECT ENG J BOYDSTON
SOLARFOX
MIDWAY MFG. CO.
FULL
1 PER
CPU SCHEMATIC
A082-90008-H000
M05H00982-A006
NOTES
A = ANALOG
E = EARTH
L = LOGIC





72 PIN TEST CONNECTOR

1	L GND	25	μA0	49	μNMI
2	+5V	26	μA1	50	μINT
3	L GND	27	μA2	51	μM1
4	+5V	28	μA3	52	μBUSACK
5	+12V	29	μA4	53	μRD
6	N.U	30	μA5	54	μWR
7	+12V	31	μA6	55	μRESET
8	VBATT	32	μA7	56	T Φ
9	μD0	33	DISDBG	57	CLKCTL
10	μD1	34	FAIL	58	μHALT
11	μD2	35	FLIP	59	μWAIT
12	μD3	36		60	HBLNK
13	μD4	37	μIORQ	61	VBLNK
14	μD5	38	μMREQ	62	
15	μD6	39	μBUSREQ	63	L GND
16	μD7	40	μRFSH	64	RED
17	VID 0	41	μA8	65	L GND
18	VID 1	42	μA9	66	GREEN
19	VID 2	43	μA10	67	L GND
20	VID 3	44	μA11	68	BLUE
21	MOVE BUF	45	μA12	69	L GND
22	INT 1	46	μA13	70	+5V
23	INT 3	47	μA14	71	L GND
24		48	μA15	72	+5V

J3		J4		J5		J6		J7	
1	L GND	1	A GND	1	L GND	1	L GND	1	mH2
2	L GND	2	A GND	2	L GND	2	BμA0	2	L GND
3	L GND	3	BμA7	3	L GND	3	L GND	3	H0
4	+5V	4	BμA6	4	+5V	4	BμD0	4	H1
5	+5V	5	BμA5	5	+5V	5	BμD1	5	H2
6	+5V	6	BμA4	6	+5V	6	BμD2	6	H3
7	N.U	7	BμA3	7	SCBMB	7	BμD3	7	H4
8	N.U	8	BμA2	8	CLK	8	BμD4	8	H5
9	N.U	9	BμA1	9	HCLK	9	BμD5	9	H6
10	BμD0	10	BμA0	10	HCLK	10	BμD6	10	H7
11	BμD1	11	+12V	11	RSELO	11	BμD7	11	H8
12	BμD2	12	+12V	12	+5V SENSE	12	L GND	12	L GND
13	BμD3	13	μWAIT	13	N.U	13	BμA0	13	VID 0
14	BμD4	14	BμIORQ	14	MOVE BUF	14	BμA1	14	VID 1
15	BμD5	15	N.U	15	634	15	BμA2	15	VID 2
16	BμD6	16	BμRD	16	DV0	16	BμA3	16	VID 3
17	BμD7	17	BμWR	17	DV1	17	BμA4	17	HSEL 0
18	N.U	18	N.U	18	DV2	18	BμA5	18	L GND
19	FLIP	19	+5V	19	DV3	19	BμA6	19	+5V
20	μRESET	20	+5V	20	DV4	20	BμA7	20	+5V
21	N.U	21	+5V	21	DV5	21	BμA8	21	+5V
22	N.U	22	L GND	22	DV6	22	L GND	22	L GND
23	N.U	23	L GND	23	DV7	23	mH0	23	L GND
24	N.U	24	L GND	24	DV8	24	mH1	24	L GND

J2	
1	RED
2	L GND
3	GREEN
4	L GND
5	BLUE
6	L GND
7	KEY
8	HBLNK
9	VBLNK

NOTES
A= ANALOG
E= EARTH
L= LOGIC
N.U= NOT USED

PROJECT ENG. A. GHOSH

m.m 06/22/82

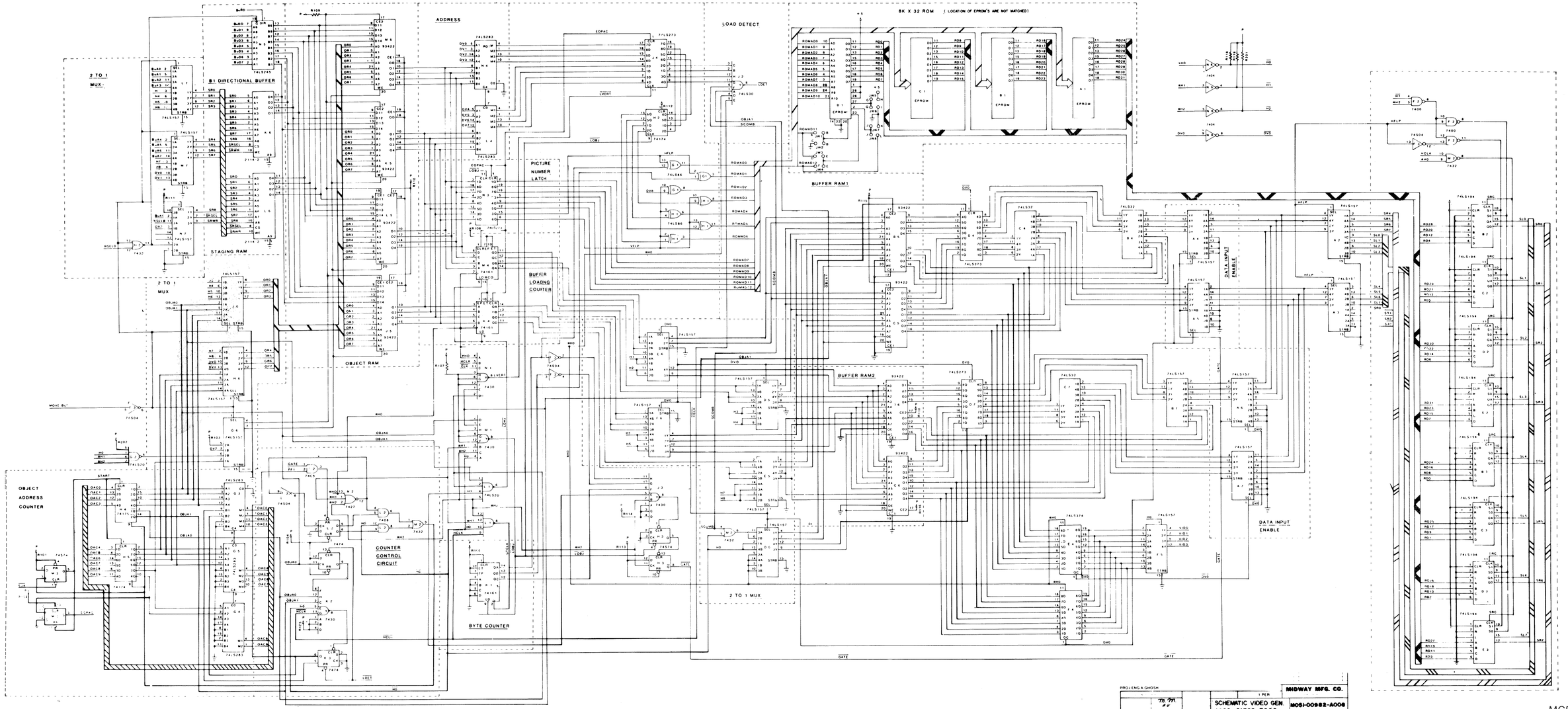
FULL | 1 PER.

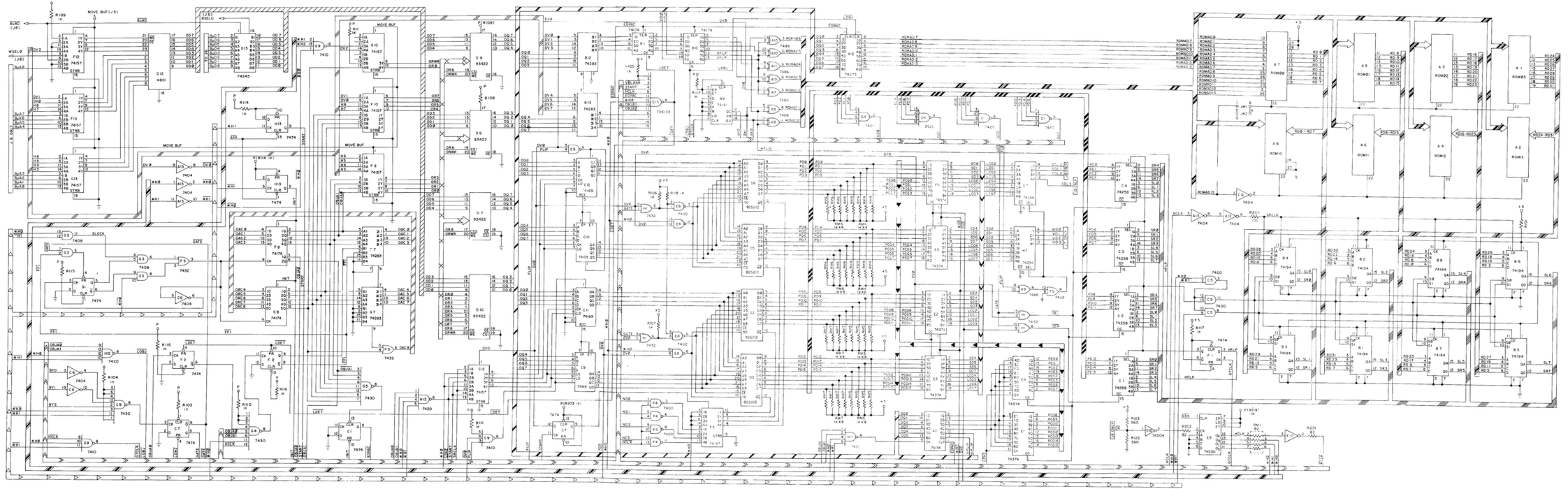
MIDWAY MFG. CO.
FRANKLIN PK. ILL.

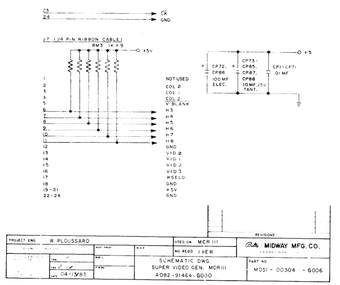
SUPER CPU SCHEMATIC DRAWING
A082-90010-C000

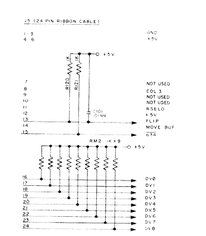
M051-00628-A008

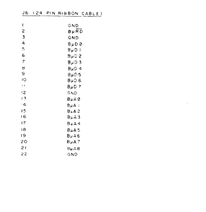
MCR-38

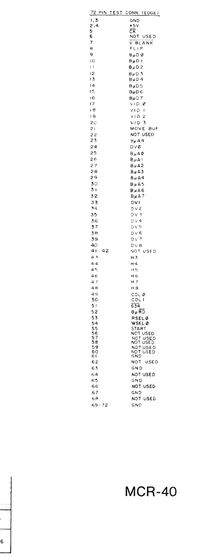

2 TO 1 MUX
B1 DIRECTIONAL BUFFER
STAGING RAM
2 TO 1 MUX
OBJECT RAM
ADDRESS
PICTURE NUMBER LATCH
BUFFER LOADING COUNTER
LOAD DETECT
8K X 32 ROM
BUFFER RAM1
BUFFER RAM2
DATA INPUT ENABLE
OBJECT ADDRESS COUNTER
COUNTER CONTROL CIRCUIT
BYTE COUNTER
2 TO 1 MUX
MIDWAY MFG. CO.
SCHEMATIC VIDEO GEN.
A082-91399-F000
MOSI-00982-A008
MCR-39

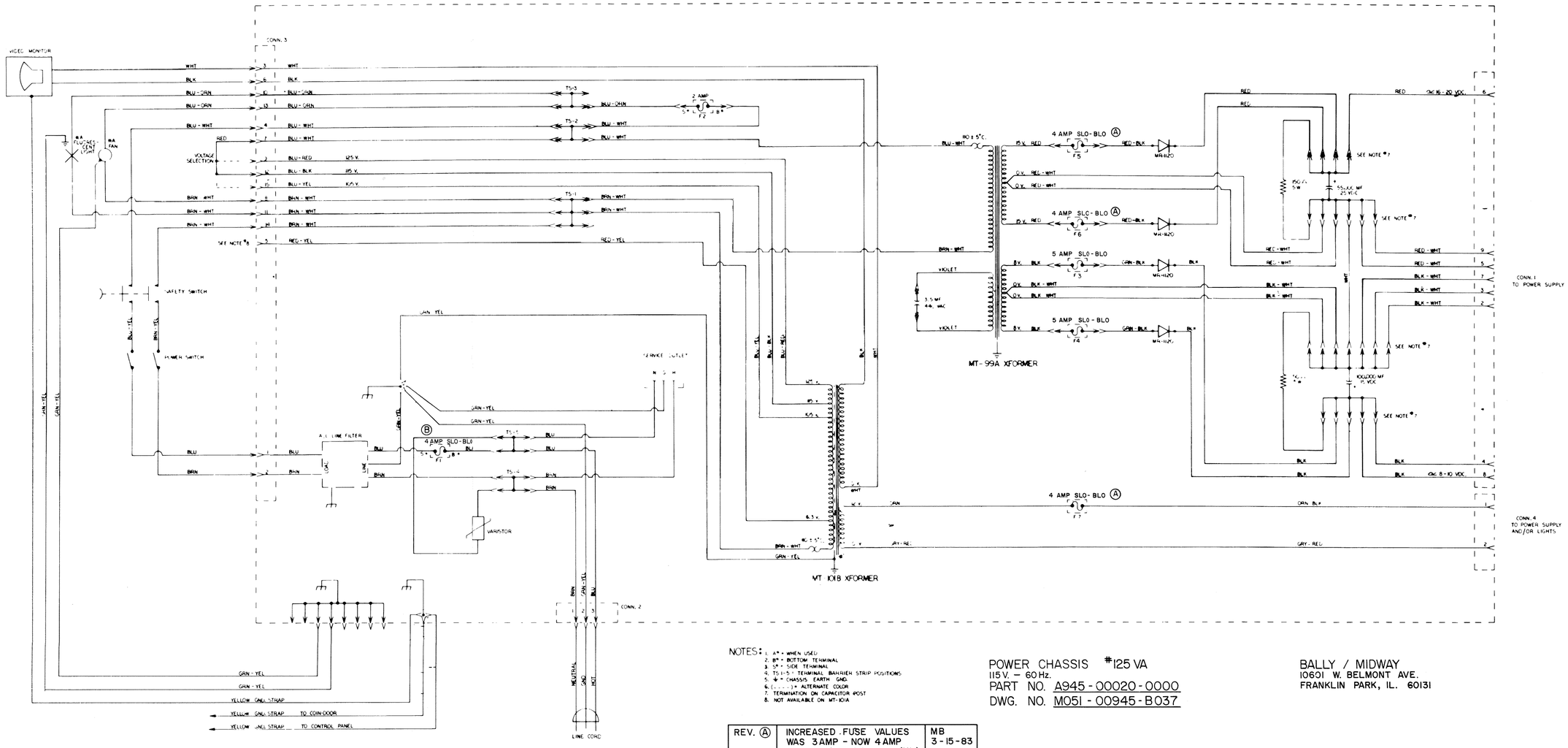










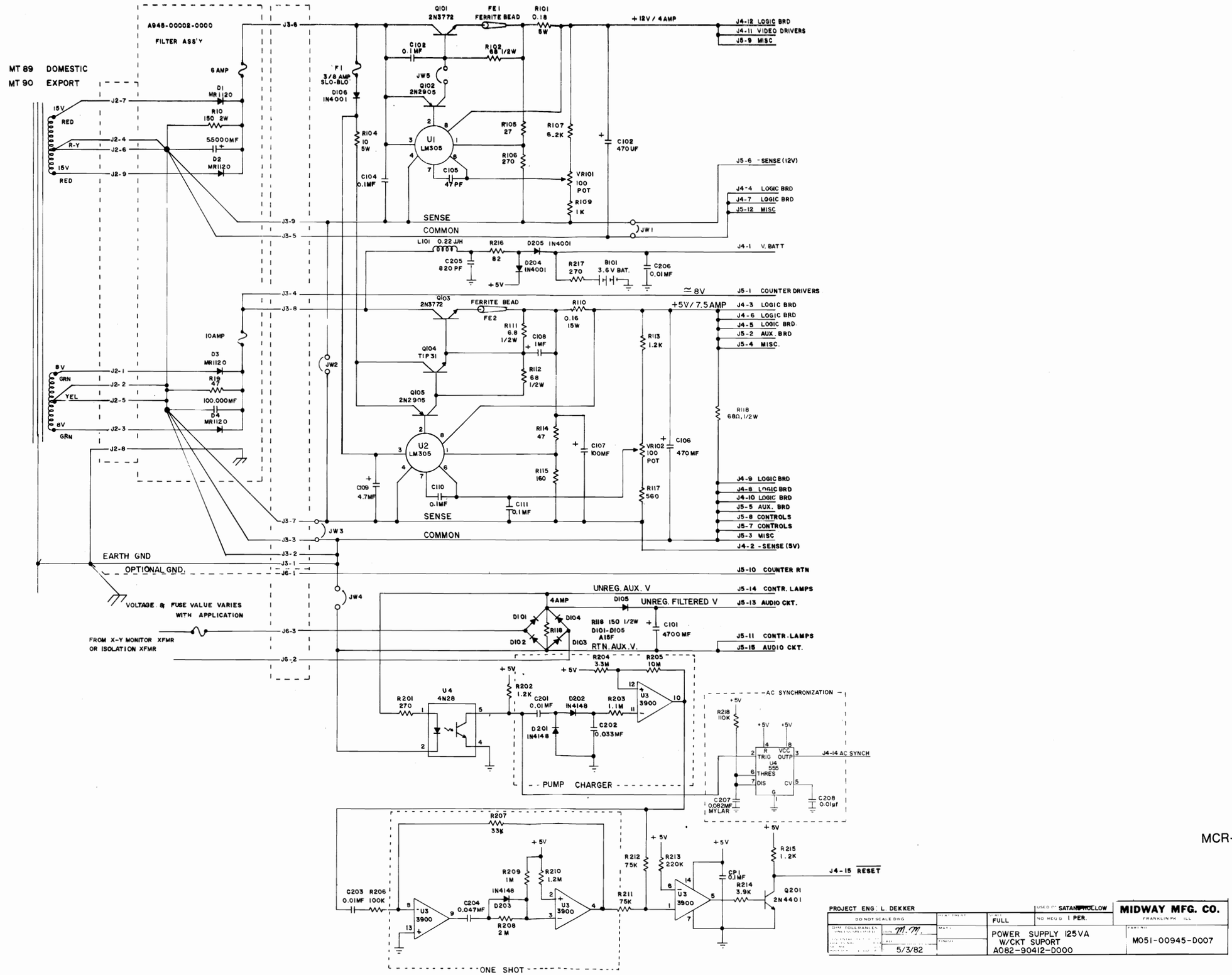


NOTES:
1. A* = WHEN USED
2. B* = BOTTOM TERMINAL
3. S* = SIDE TERMINAL
4. TS 1-5 = TERMINAL BARRIER STRIP POSITIONS
5. ⏚ = CHASSIS EARTH GND.
6. (_ _ _) = ALTERNATE COLOR
7. TERMINATION ON CAPACITOR POST
8. NOT AVAILABLE ON MT-101A

REV. Ⓐ	INCREASED FUSE VALUES WAS 3 AMP - NOW 4 AMP ADDED PART NO. (UL)	MB 3-15-83
REV. Ⓑ	INCREASED FUSE VALUE WAS 3AMP – NOW 4 AMP	MB 3-24-83

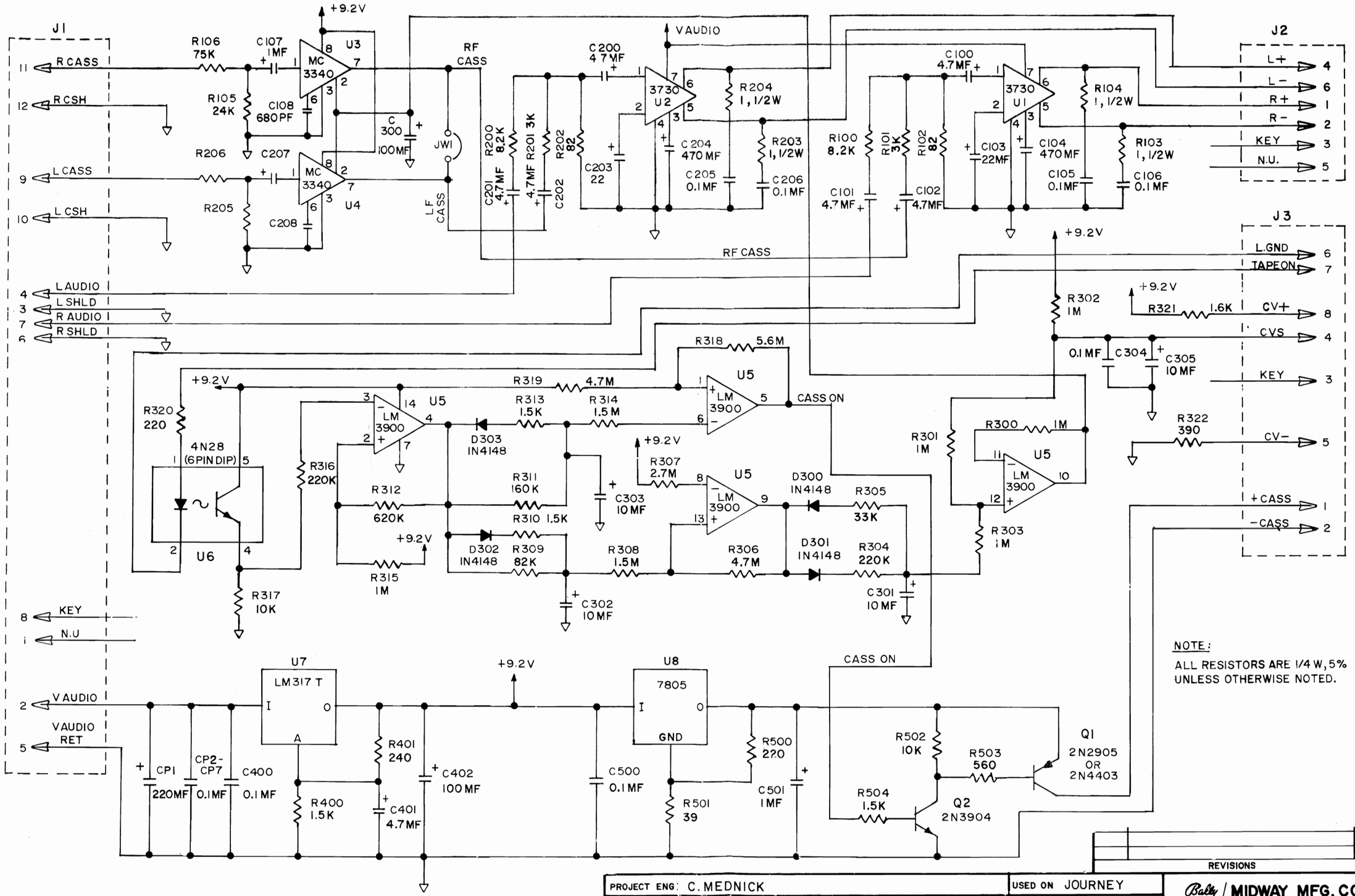
POWER CHASSIS #125 VA
115 V. – 60 Hz.
PART NO. A945-00020-0000
DWG. NO. M051-00945-B037

BALLY / MIDWAY
10601 W. BELMONT AVE.
FRANKLIN PARK, IL. 60131



MCR-42

PROJECT ENG: L. DEKKER
DO NOT SCALE DRG.
USED ON: SATAN/HOLLOW
FULL
NO REQ'D 1 PER.
MIDWAY MFG. CO.
FRANKLIN PK ILL.
5/3/82
POWER SUPPLY 125VA W/CKT SUPORT
A082-90412-D000
M051-00945-D007

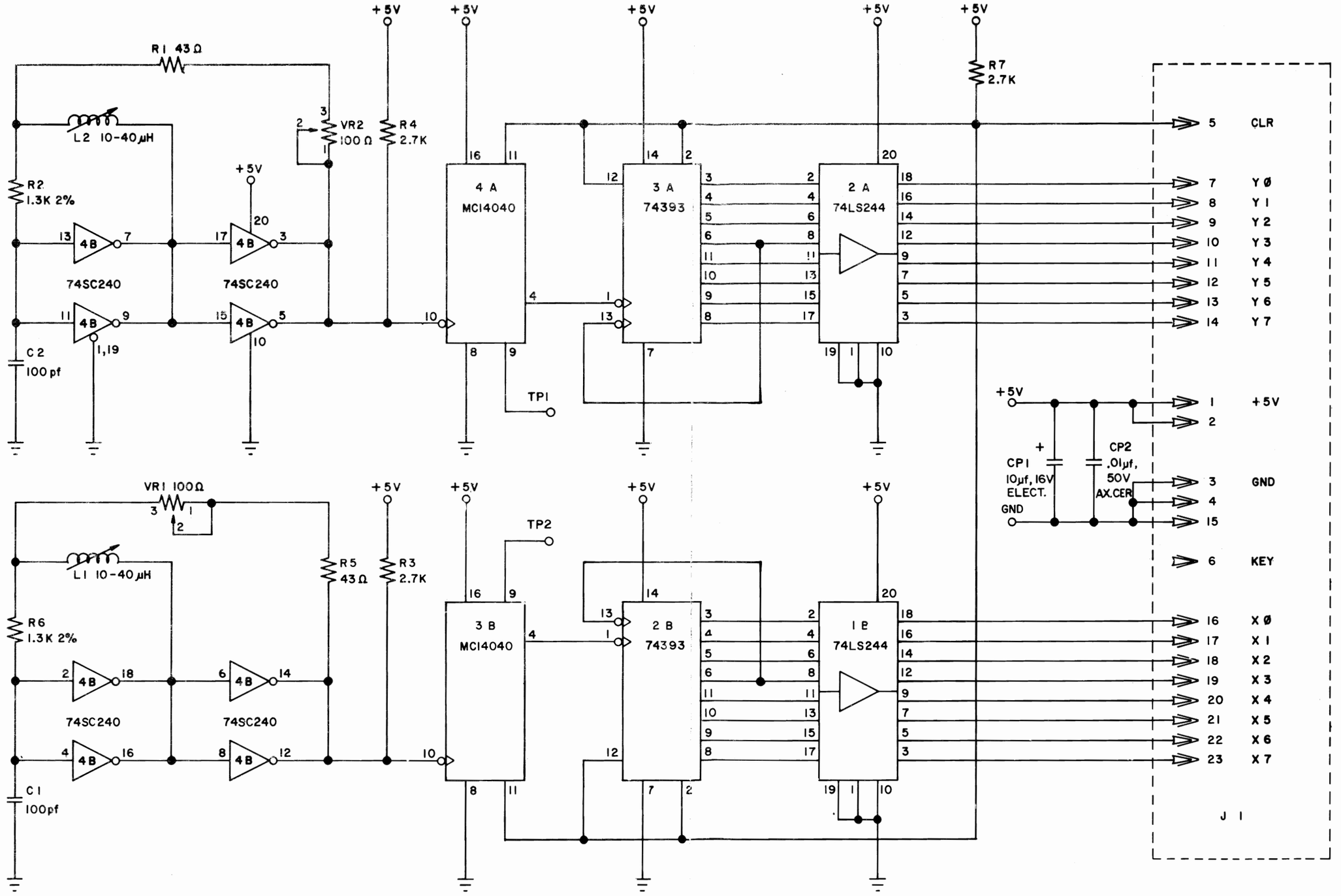


NOTE:

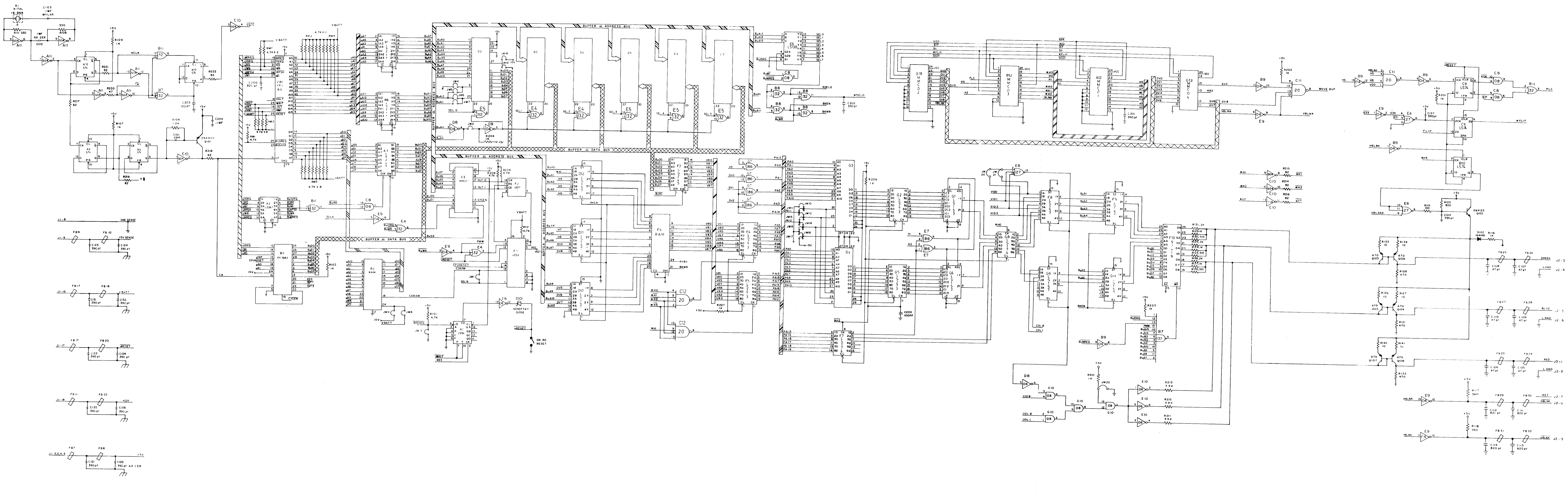
ALL RESISTORS ARE 1/4 W, 5% UNLESS OTHERWISE NOTED.

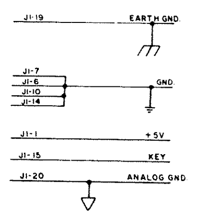
REVISIONS

PROJECT ENG: C. MEDNICK			USED ON JOURNEY	Bally / MIDWAY MFG. CO. FRANKLIN PK. ILL.
DO NOT SCALE DWG.	HEAT TREAT	SCALE FULL	NO. REQ'D 1PER	
DIM. TOLERANCES UNLESS SPECIFIED CONCENTRICITY T.I.R. .005 FRACTIONAL ±1/64 DECIMAL .015 HOLE DIA +.002 .000	DRN. T&B CKD. DATE 04/07/83	MAT'L. FINISH	DUAL PWR AMP W/CASS INTERFACE SCHEMATIC DWG A084-91496-B358	PART NO. M051 - 00358 - B009



PROJECT ENG: JOHN BOYDSTON			USED ON KOZMIK KROOZ'R	Bally / MIDWAY MFG. CO. FRANKLIN PK. ILL.
DO NOT SCALE DWG.	HEAT TREAT	SCALE FULL	NO. REQ'D 1 PER	
DIM. TOLERANCES UNLESS SPECIFIED CONCENTRICITY T.I.R .003 FRACTIONAL ± 1/64 DECIMAL ± .005 HOLE DIA +.002 -.000	DRN. C.C CKD. JBS DATE 2/17/83	MAT'L. FINISH	SCHEMATIC DWG, ANALOG JOYSTIC P.C. A082-91458-E000 A084-91458-E000	PART NO. M051-00986-E024





72 PIN TEST CONNECTOR

1	L GND	25	uA0	49	uNMI
2	+5V	26	uA1	50	uINT
3	L GND	27	uA2	51	uMI
4	+5V	28	uA3	52	uBUSACK
5	+12V	29	uA4	53	uRD
6	N.U	30	uA5	54	uWR
7	+12V	31	uA6	55	uRESET
8	VBATT	32	uA7	56	T∅
9	uD0	33	DISDOG	57	N.U.
10	uD1	34	N.U.	58	uHALT
11	uD2	35	FLIP	59	uWAIT
12	uD3	36	N.U.	60	HBLNK
13	uD4	37	uIORQ	61	VBLNK
14	uD5	38	uMREQ	62	N.U.
15	uD6	39	uBUSREQ	63	L GND
16	uD7	40	uRFSH	64	RED
17	VID 0	41	uA8	65	L GND
18	VID 1	42	uA9	66	GREEN
19	VID 2	43	uA10	67	L GND
20	VID 3	44	uA11	68	BLUE
21	MOVE BUF	45	uA12	69	L GND
22	INT 1	46	uA13	70	+5V
23	INT 3	47	uA14	71	L GND
24		48	uA15	72	+5V

J3		J4		J5		J6		J7		J2	
1	L GND	1	A GND	1	L GND	1	L GND	1	N.U.	1	RED
2	L GND	2	A GND	2	L GND	2	BuRD	2	COL ∅	2	L GND
3	L GND	3	BuA7	3	L GND	3	L GND	3	COL 1	3	GREEN
4	+5V	4	BuA6	4	+5V	4	BuD∅	4	N.U.	4	L GND
5	+5V	5	BuA5	5	+5V	5	BuD1	5	VBLANK	5	BLUE
6	+5V	6	BuA4	6	+5V	6	BuD2	6	H3	6	L GND
7	N.U	7	BuA3	7	N.U.	7	BuD3	7	H4	7	KEY
8	N.U	8	BuA2	8	N.U	8	BuD4	8	H5	8	HBLNK
9	N.U	9	BuA1	9	N.U.	9	BuD5	9	H6	9	VBLNK
10	BuD0	10	BuA0	10	N.U	10	BuD6	10	H7		
11	BuD1	11	+12V	11	RSEL0	11	BuD7	11	H8		
12	BuD2	12	+12V	12	+5V SENSE	12	L GND	12	L GND		
13	BuD3	13	uWAIT	13	FLIP	13	BuA0	13	VID 0		
14	BuD4	14	BuIORQ	14	MOVE BUF	14	BuA1	14	VID 1		
15	BuD5	15	N.U.	15	634	15	BuA2	15	VID 2		
16	BuD6	16	BuRD	16	DV0	16	BuA3	16	VID 3		
17	BuD7	17	BuWR	17	DV1	17	BuA4	17	WSEL0		
18	N.U.	18	N.U.	18	DV2	18	BuA5	18	N.U.		
19	FLIP	19	+5V	19	DV3	19	BuA6	19	+5V		
20	uRESET	20	+5V	20	DV4	20	BuA7	20	+5V		
21	N.U	21	+5V	21	DV5	21	BuA8	21	+5V		
22	N.U	22	L GND	22	DV6	22	L GND	22	L GND		
23	N.U.	23	L GND	23	DV7	23	CK	23	L GND		
24	N.U.	24	L GND	24	DV8	24	L GND	24	L GND		

NOTES
A = ANALOG
E = EARTH
L = LOGIC
N.U. = NOT USED

PROJECT ENG R.A. PLOUSSARD		USED ON JOURNEY		Bally / MIDWAY MFG. CO. FRANKLIN PK. ILL
DO NOT SCALE DWG		SCALE FULL	NO REQ'D 1 (ONE)	REVISIONS
DWN 180	CHK RGP	DATE 04/15/83	SUPER CPU MCR III SCHEMATIC DWG A082-91475-D000	PART NO M051-00304-D008

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