part 3

The Williams Game

The Williams' electronic pinball game has undergone a fair bit of evolution since its earlier versions. It has a very capable processing system featuring lots of processing power and includes a second microcomputer dedicated solely to sound generation. The same system has also been adapted for use in Williams' Shuffle Alley games.

There are five major boards in the Williams pinball system. The first is the master display board which contains the driver circuits for the five displays and is mounted on the insert board in the backbox. The next two are in the backbox on the left-hand side. The upper one is the CPU board and the lower is the driver board. The CPU (central processing unit) board contains most of the microcomputer and outputs to the master display board, while the driver board contains the rest of the microcomputer I/O ports. These control the driving circuitry for the switch matrix, lamp matrix, and solenoids. The outputs to the sound board are tapped off the solenoid driver outputs. The microcomputer bus connects to the driver board via connector 1J1.

The fourth board, in the middle right hand side of the backbox, is the power supply board containing some of the game's fuses, the two display regulators, the +5 volt logic regulator, and some additional components of the other supplies.

Below the power supply board is mounted the fuse card which holds the fuses for the general illumination supply and the +5 volt logic regulator. To the right are two rectifier bridges, one for the solenoid supply and the other for the switched lamp supply. The large capacitor mounted on the bottom of the backbox is the switched lamp filter capacitor.

The fifth board is the sound board located directly above the power supply module. In earlier games this board was located in the cabinet beside the tilt assemblies and line filter.

Connectors in the Williams game have a prefix indicating the board or circuit area, then a "P" or a "J" to indicate a male or female side, and then the pin number. Example: "3P4".

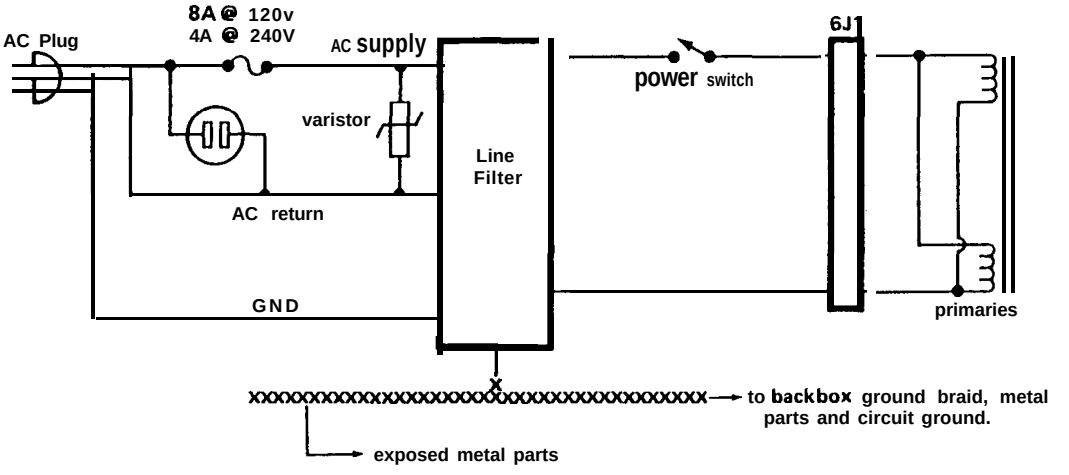
1. POWER SUPPLIES

Primary Circuits

Power enters the Williams game through an AC cord connected to the wooden side board in the cabinet. The supply side connects first to the 8 ampere fast-blow (4 ampere if operated at 220 volts AC) primary fuse and then the line filter. A 130 volt rms (275Vrms at 220 volts) varistor is wired across the input to the line filter to prevent voltage spikes from entering or leaving the game. The auxiliary AC receptacle is wired across the AC cord before the fuse and allows for connection of trouble lights, etc. The hot side of the supply, after the line filter, leads to the power switch and then connects to the power transformer in the backbox via connector 6P1 together with the AC return wire. The primaries can be connected differently to the supply wires for line voltages of 105V, 117V, 210V and 235V AC. Refer to the Williams schematics for detailed information.

An earth ground braid wire is connected to ground via the line filter. The braid connects to all external metal parts except for the ventilation hole screens. Part of the braid connects to the backbox for grounding the circuits in the backbox and metal parts. All the circuit boards connect to ground, via their mounts and the ground braid wire, with their own mounting screws. There is no direct wire connection from the AC cord

ground to the boards themselves. This means that the cabinet braid wire must be connected to ensure proper grounding.



Secondary Supplies

There are five secondary supplies in the Williams games. These are the 6.3V AC supply for general illumination, the filtered +18V supply for the lamp matrix, the +28V supply for the solenoids, the 90V AC supply which is rectified, filtered, and regulated to provide the +100V and -lOOV supplies for the displays, and the 18.6V AC centre tapped supply. This latter supply is also regulated but to +5V for the game logic and to +12V and –12V for the sound module. These are illustrated on page 3-4.

The 6.3V AC secondary wires from the transformer are soldered directly to the fuse card located below the power supply board. The supply side is fused with a 20A fast-blow fuse. Two pair of supply and return wires provide lamp power to the insert board. Another pair of wires provides illumination to the playfield and a fourth pair provides power to the coin slot bulbs.

The next secondary provides the +18V DC power to the lamp matrix. It is full-wave rectified by the 35A 100PIV bridge rectifier to the lower right of the power supply board and filtered by the large 30,000μF, 25V electrolytic can capacitor mounted to the left of the power transformer (note that this capacitor has been incorrectly labelled 12,000 μF in the past). Fuse protection is provided by F3, an 8A fast-blow fuse, located on the power supply board. If the rectifier or capacitor shorts out, the primary fuse will blow.

The 25V AC secondary is full-wave rectified by the second 35A 100PIV rectifier bridge beside the lamp rectifier providing the +28V for the solenoids. A wire from the solenoid rectifier leads to the power supply board. Here a 0.1μF, 500V disc capacitor, 100μF,100V electrolytic capacitor, and a 30Vrms varistor are wired across the supply outputs. These help control any voltage spikes generated by the solenoids and not de-

spiked because of bad despiking diodes on the coils. The 100μF capacitor gives the coils much more punch when they are first energized. Any shorts in the rectifiers, the capacitors, or varistor should blow the primary fuse.

The flipper coils have their own 10A fast-blow fuse (15A for four flipper games) located on the power supply board. In earlier games, a second wire from the solenoid rectifier led, through a 1 pin connector, directly to the flipper fuse located under the playfield.

The solenoid supply is also protected by a second fuse, F2, a 2.5 ampere slow-blow fuse located on the power supply board. Two wires leave the board to the rest of the game. One provides power to the knocker and coin lockout coils in the cabinet, and the second provides power to the other coils under the play-field.

There are seven solenoid return wires which connect to the driver board via connector 2J10, on the left hand side of the driver module.

The fourth secondary supply provides power to the display regulators. It is fused with F1, a %A slow-blow fuse, located on the power supply board. The outputs of these regulators are +100 volts, -100 volts and -300 volts with the latter output being used only in the earliest games.

The fifth secondary is centre tapped and provides power to the +5 volt regulator on the power supply board and to the separate supplies on the sound board. This latter board has its own +5 volt regulator and unregulated +12V and -12V supplies.

The centre tap is ground referenced in both the power supply board and sound board. The regulator module is fused with 4A slow-blow fuses mounted on the fuse card (not found in earlier games). F5 is a 4A slow-blow fuse located after the regulator's rectifiers on the power supply board. Both sides of the supply leading to the sound board are fused with 4A slow-blow fuses on the sound board itself. In earlier games, F2 was located beside the sound board in the cabinet, not on the module.

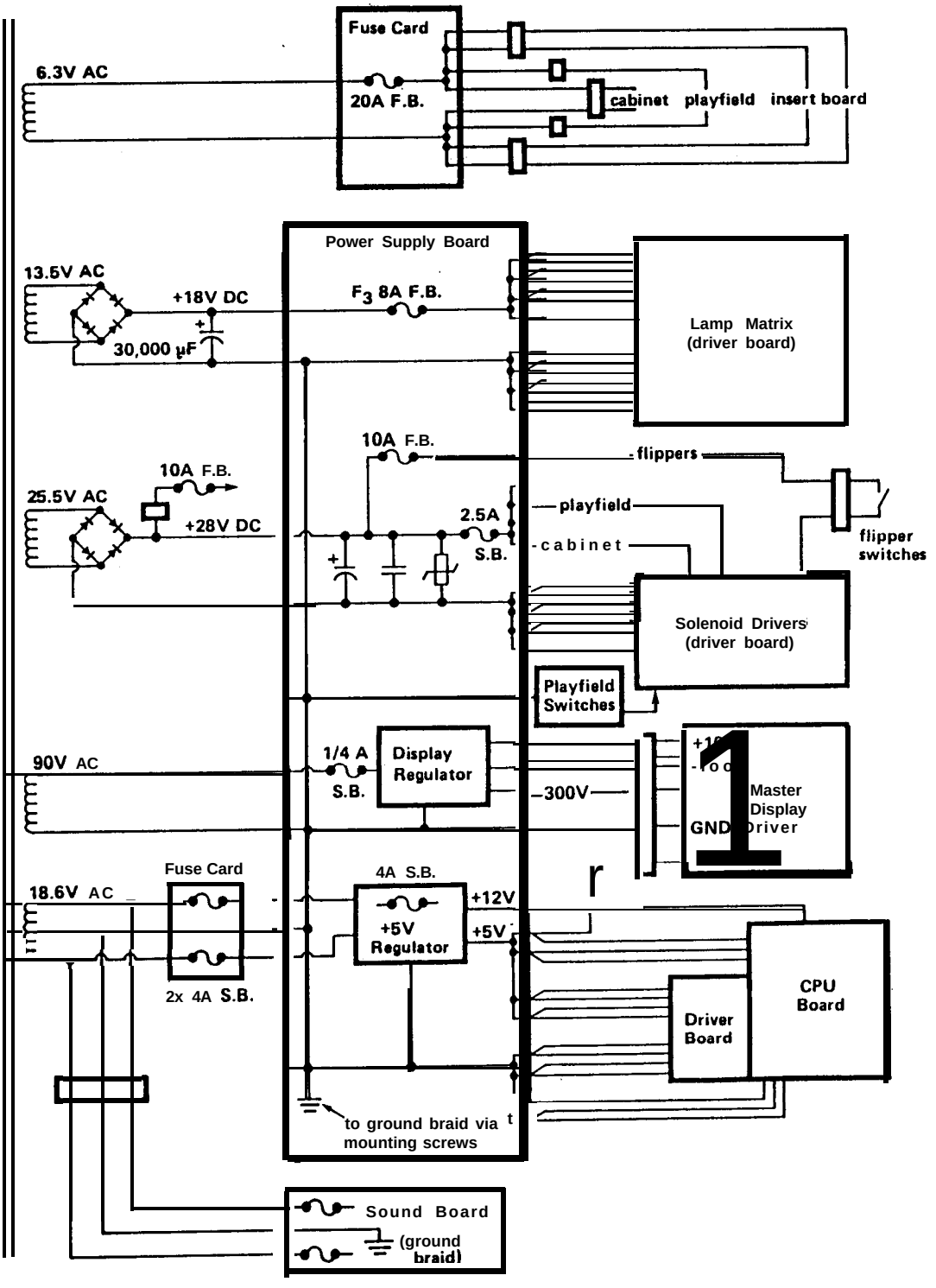
The lead from the filter capacitor of the +5 volt regulator on the power supply board is called "+12V", although its actual voltage may fluctuate between 9 and 12 volts depending upon the line voltage in the area. It is monitorred by the CPU board to detect power-up and power-down in the system.

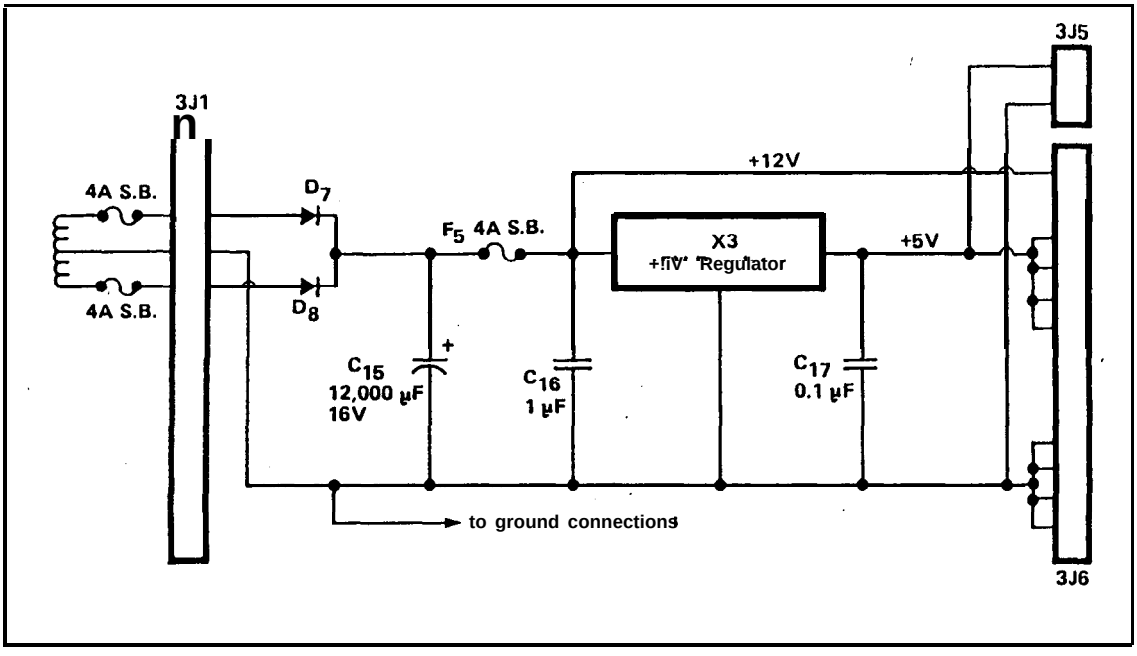
The +5 volt output from the power supply board connects to the master display driver board over one wire, to the CPU board over three wires, and to the driver board over four wires. Similarly there are seven return wires.

Special care should be taken with the plastic strip protecting the edge of the transformer shield. The metal has very sharp edges which can cut into any of the wires easily and short them to ground.

+5 Volt Regulator

The main 5 volt regulator is based around a fully integrated regulator chip at X3 on the power supply board. The 18.6 volt AC supply is fused by two 4A fuses mounted on the fuse card below the power supply board and is then full-wave rectified by the two MR500 types diodes D7 and D8. (As mentioned above, earlier games did not have these fuses.) Filter capacitor Cl5 is a 12,000μF capacitor rated at 16V DC. With no load, there is no ripple voltage, and the capacitor is charged up to around 12 volts.


Fuse Card
6.3V AC
20A F.B.
cabinet
playfield
insert board
Power Supply Board
13.5V AC
+18V DC
F3 8A F.B.
30,000 µF
Lamp Matrix
(driver board)
10A F.B.
flippers
10A F.B.
25.5V AC
+28V DC
2.5A
S.B.
playfield
cabinet
flipper
switches
Solenoid Drivers
(driver board)
Playfield
Switches
90V AC
1/4 A
S.B.
Display
Regulator
-300V
Master
Display
Driver
GND
Fuse Card
18.6V AC
4A S.B.
+12V
+5V
+5V
Regulator
2x 4A S.B.
CPU
Board
Driver
Board
to ground braid via
mounting screws
Sound Board
(ground
braid)



The logic supply fuse, F5, is rated at 4A and is a slow-blow type. In earlier games, this is the only fuse used in this supply. Capacitors Cl6 and Cl7 act as high frequency bypass capacitors and help prevent oscillation of the regulator. X3 may be replaced with an LM323K, LAS1405, or 78H05KC regulator.

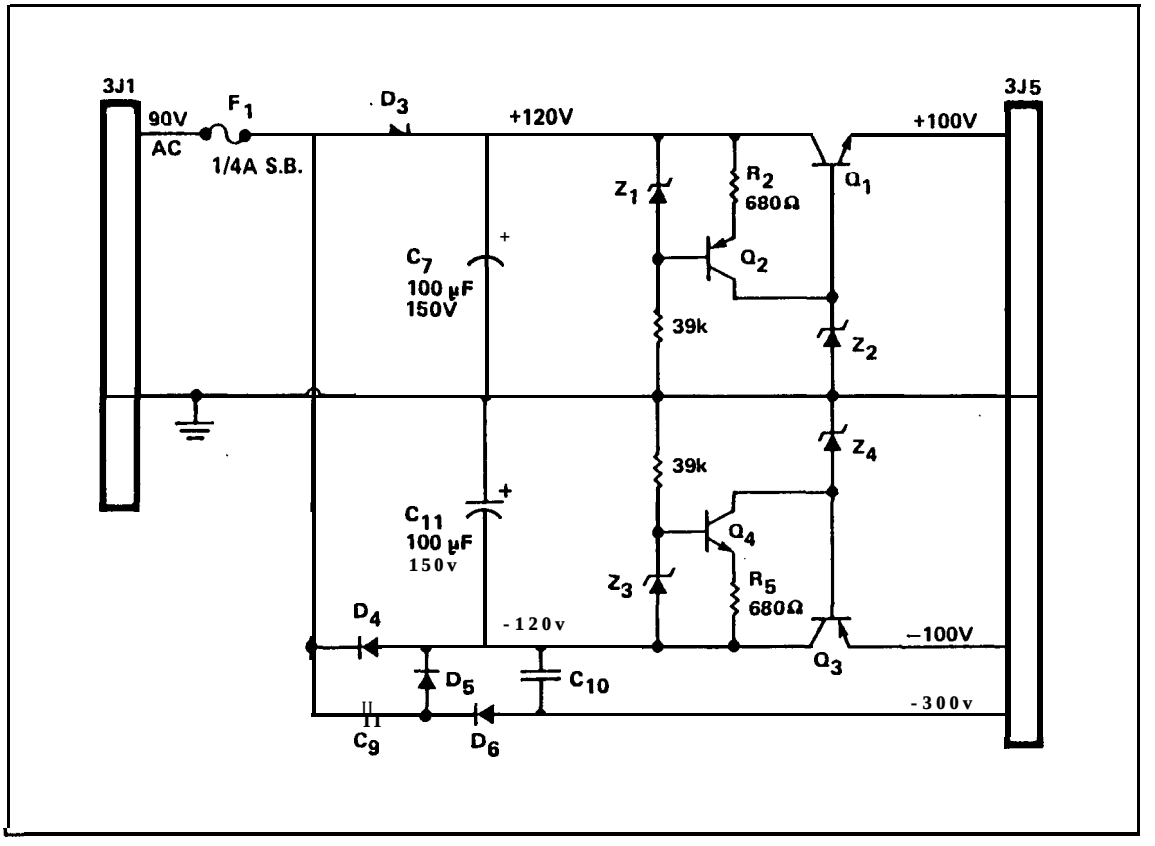
Display Regulators

The display regulators are located on the power supply board. Both function similarly, but with opposite polarity. The circuit is protected with F1, a 1/4 ampere, slow-blow fuse. The supply is half-wave rectified for the positive supply and half-wave rectified for the negative supply by 1 N4004 type diodes D3 and D4. The supplies are filtered by their own 100 μF, 150 volt capacitors C7 and Cl 1 which charge up to around +120V and -120V respectively with no load.

Short circuit protection is accomplished in the regulators by providing a constant base current supply for the pass transistors. This base current is defined by Q2, Z1 and R2 in the positive regulator and Q4, Z3, and R5 in the negative regulator which act as the constant current sources.

Z1 and Z3 are both 1 N5990B 3.9 volt Zener diodes. The emitter of Q2 is 0.6 volts higher than its base voltage, and the emitter of Q4 is 0.6 volts lower than its base, meaning that 3.3 volts is applied across R2 and R5. Current flow, then, will be I = E/R = 3.3V/680Ω = 4.9mA. Most of this current is collector current which can flow through either the 100 volt Zener diodes Z2 and Z4 or through the series pass transistors Q1 and Q3.

Under no load conditions, the output of the regulator is open and so there can be no base current. The 1 OOV 1 N4764A Zener diodes Z2 and Z4 then conduct the collector current of Q2 and Q4 to ground. The heat produced in the Zeners is 4.9mA x 100V or 1/2 watt. The Zener diodes specified are rated at 1 watt to ensure reliability.



Under heavier load conditions, such as when the displays are drawing current, the emitter voltages of the pass transistors tend to drop a bit, increasing the emitter-base forward bias voltage drops. This also tends to pull the base voltage of Q1 a little lower and the base voltage of Q3 a little higher, diverting the collector currents of Q2 and Q4 away from the 100 volt Zeners. When load current increases to the point that Z2 or Z4 current is zero, further increases in loadipq will result in the collector voltage of Q2 decreasing or the collector voltage of Q4 increasing. The pass transistors have limited amounts of current gain, so that even with a steady 5mA of base current, their collector current won't surpass more than about 0.2 amps, depending upon the individual transistors. If both regulators short at the same time, F1 will blow.

Q1 should be replaced with a Motorola type SDS201 NPN transistor and Q3 with a type SDS202 PNP transistor.

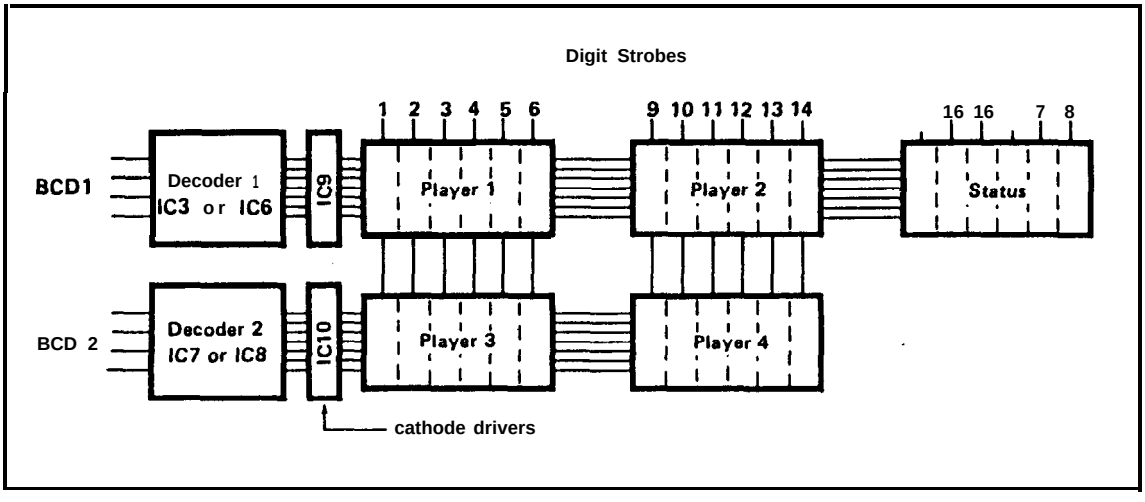
D4, D5, D6, C9 and Cl0 are intended to function as a voltage triplet-. Diode D5 prevents the output side of C9 from increasing above the filter capacitor voltage of about -125 volts. However, C9 AC couples the full peak to peak voltage of the AC supply to D6 which charges C10. The voltage on Cl0 will be equal to the ripple voltage on Cl 1 plus the peak-to-peak AC voltage of the supply. This will be (–120V) + (–240V) = -360 volts. However, the efficiency of this type of circuit is poor and the output voltage is more likely to be around -320 volts.

The -300 volt supply was used in the earlier games to help ionize the gas in the display tubes but is not used in present displays.

2. MASTER DISPLAY DRIVER BOARD

The master display driver board provides the decoding and driving functions for the five 6 digit, seven segment gas discharge display tubes. The CPU board provides 16 digit strobes and two sets of BCD data to the master display driver. The displays are matrixed with BCD data group 1 controlling the cathode segments of players 1 and 2 and the status displays and with BCD data group 2 controlling players 3 and 4.

Digit strobes 1 through 6 control player 1 and 3 digit anodes, starting with the 100,000s column as digit strobe 1. Digits 9 through 14 control the 2nd and 4th player digits, and digits 15, 16, 7, and 8 control the status display.



There are two types of master display boards used by Williams. The earlier type used IC drivers while the newer ones use discrete transistor drivers. The switch-over grew out of problems Williams had in obtaining sufficient quantities of their IC drivers. We will look at the earlier system first.

Old Display Driver Board

There are four types of integrated circuits used on the earlier board. These are the digit drivers, segment drivers, BCD to 7 segment decoders, and CMOS inverters. Provision was made to allow the replacement of the first three parts with alternate parts in the event of difficulty in obtaining parts.

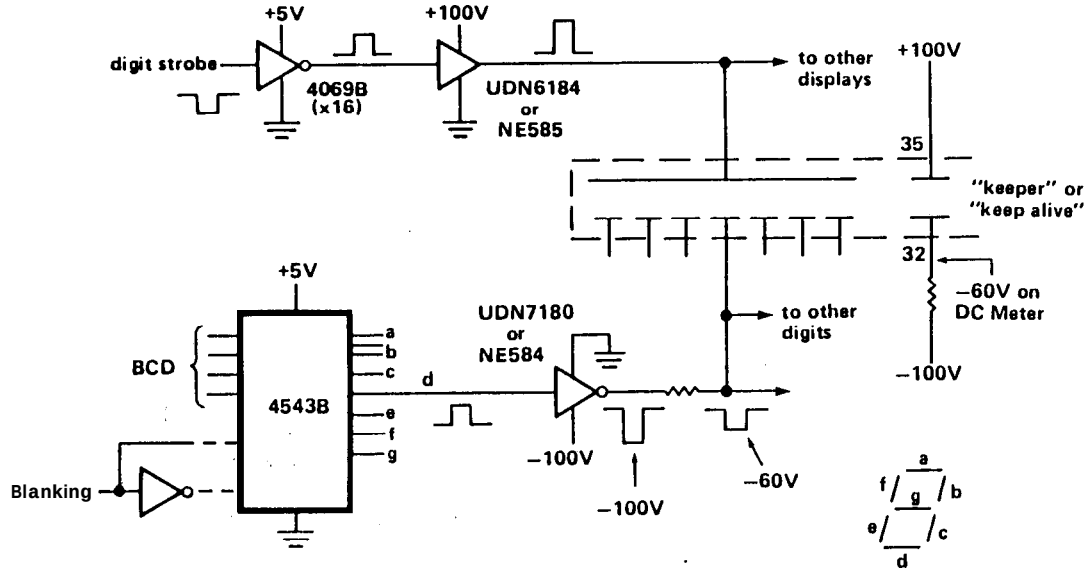
Either a Sprague UDN6184 or Signetics NE585 octal anode driver, or equivalent, may be used in locations IC4, IC11, IC12, or IC13. The NE585 are 22 pin chips and require ZR1, a 1N6000B10 volt Zener diode and resistor R22 if one or more of these parts are used. The UDN6184s are 20 pin chips and are not affected by the use of ZR1.

Either a Sprague UDN7180 or Signetics NE584 octal cathode driver, or equivalent, may be used in locations IC9 or IC10. The NE584 requires a 91 k pull-down resistor on pin 12 on each of these chips that may be used. These are 22 pin parts. The UDN7180 is a 20 pin device.

The two possible BCD to seven segment decoders which can be used are both 16 pin CMOS parts but have different pins used for inputs and outputs. The 45438 is used in locations IC5 and IC8. The 45588 can be used in locations IC6 and IC7. The different locations have the traces connected differently to take into account the pin differences. As the segment patterns for the three digits "1", "6", and "9" are output differently in the two decoders, it is recommended that only one type of decoder be used in each board.

The fourth type of part is the CMOS 40698 inverters located at IC1, IC2 and IC3. These are used to invert the digit strobe data from the CPU board and invert the blanking signal for the 45438 type decoder chip. The Blanking line turns off the displays in the event of a malfunction on the CPU board as well as during power-up and power-down.

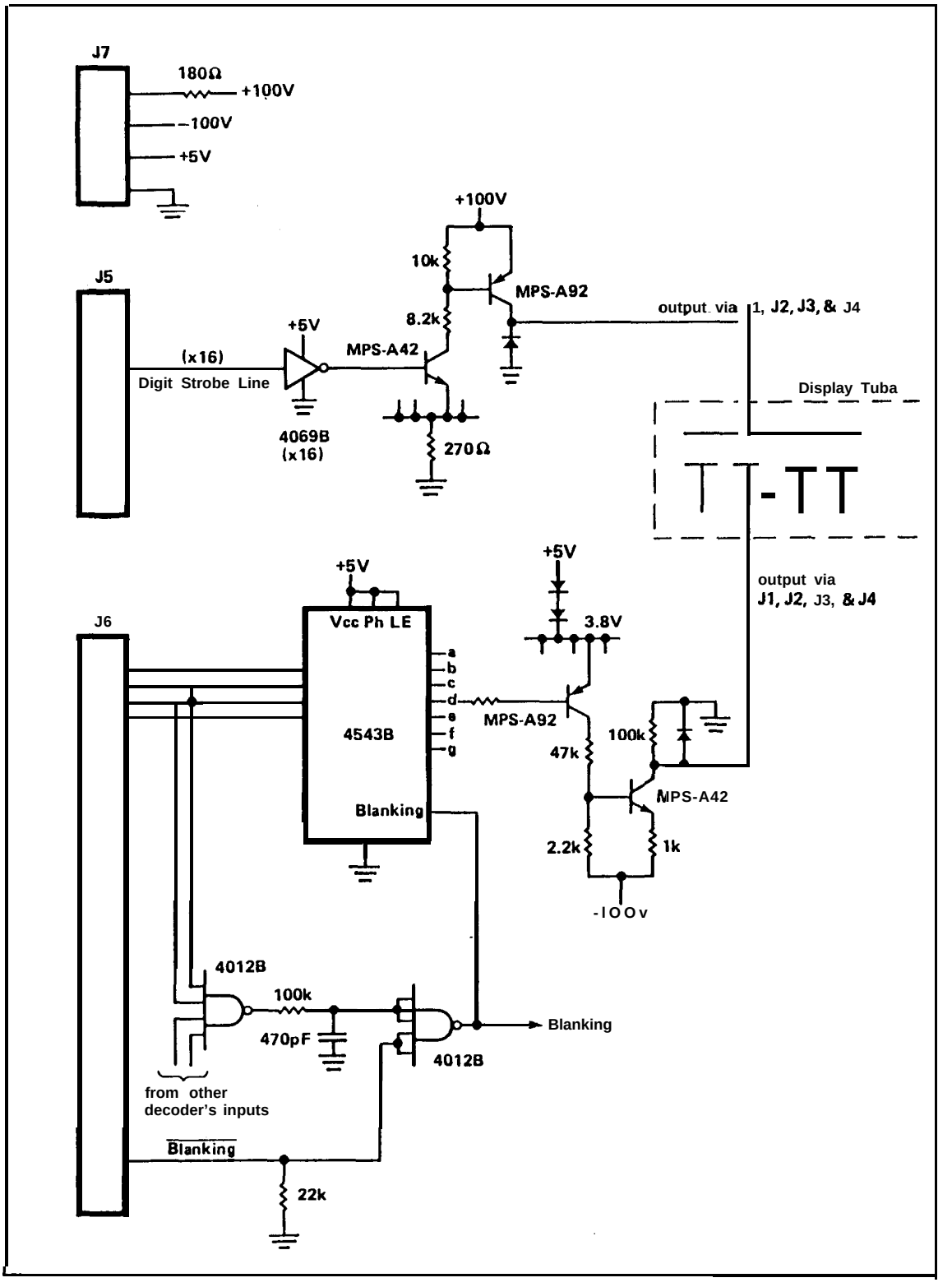
The digit drivers act as buffer amplifiers, whereas the segment (cathode) drivers act as inverters.



New Display Driver Board

The block layout of the newer master display board is similar to the layout of the older board but with several important differences.

Sixteen 4069B CMOS inverters are used as input inverting buffers from the CPU board for the digit strobes. An MPS-A42 transistor inverts the output from each gate and acts as a level shifter for the MPS-A92 driver. Since only one of the level shifter transistors is on at a time, one single 270Ω resistor is shared between all sixteen of the transistors. This lets the outputs of the CMOS inverters go HIGH, yet still allows the transistors' to maintain a 0.6V drop from base to emitter.


J7
180Ω
+100V
-100V
+5V
+100V
10k
MPS-A92
J5
8.2k
output via J1, J2, J3, & J4
+5V
(x16)
MPS-A42
Digit Strobe Line
Display Tuba
4069B
(x16)
270Ω
+5V
+5V
J6
Vcc Ph LE
3.8V
a
b
c
d
e
f
g
MPS-A92
4543B
100k
47k
MPS-A42
Blanking
2.2k
1k
-100v
4012B
100k
Blanking
470pF
4012B
from other
decoder's inputs
Blanking
22k

The 8.2k and 10k resistors are used to turn ON and turn OFF, respectively, the MPS-A92 driver. The clamp diode on the driver's collector protects the transistor from exposure to negative voltage spikes which may be applied to the anode due to the negative voltages on the segment cathodes in the display tube.

The cathode drivers are controlled by the segment output pins of the 45438 decoders. The emitter supply for the fourteen MPS-A92 level shifters in this circuit is at t3.8 volts and is derived from the +5V logic supply through two silicon diodes. Since the 45438's output HIGH voltage is close to t5 volts, this guarantees quick turn OFF of the A92s. The 47k and 2.2k resistors, respectively, turn ON and OFF the MPS-A42 segment drivers. When the level shifter transistor is turned ON, its collector voltage is approximately +3.4V. The 47k and 2.2k resistors now have 103.4 volts across them and divide this to about -95.4 volts at the driver's base, which is 4.6 volts higher than the -lOOV supply. Allowing for the emitter base drop, the 1 k resistor has about 4 volts across itself with a current of I= E x R, or about 4mA, through it. This of course makes this a current switching circuit rather than a voltage switching circuit.

The 100k resistor from the driver's collector to ground helps to discharge the small amount of cathode and transistor capacitance to ground. The clamp diode protects the driver against positive voltage spikes contributed by the anode drivers through the display tube.

A 40128 CMOS dual 4-input NAND gate is used on this board to control the blanking inputs of the 45438 decoders. If the Blanking signal from the CPU board goes LOW, or if the connectors are disconnected from the CPU board, the blanking inputs on the decoder are raised HIGH, turning OFF all the displays.

The other 4-input NAND gate connects to the 8s and 4s inputs of both decoders. If the CPU board sends out all HIGHs on these lines, between strobe signals, (corresponding to decimal values of twelve or higher), the blanking inputs are also raised HIGH, turning OFF the decoders. The combination 100k resistor and 470pF capacitor prolongs the decoders' blanking signal until all the BCD data is latched into the master display board and the digits are set up again.

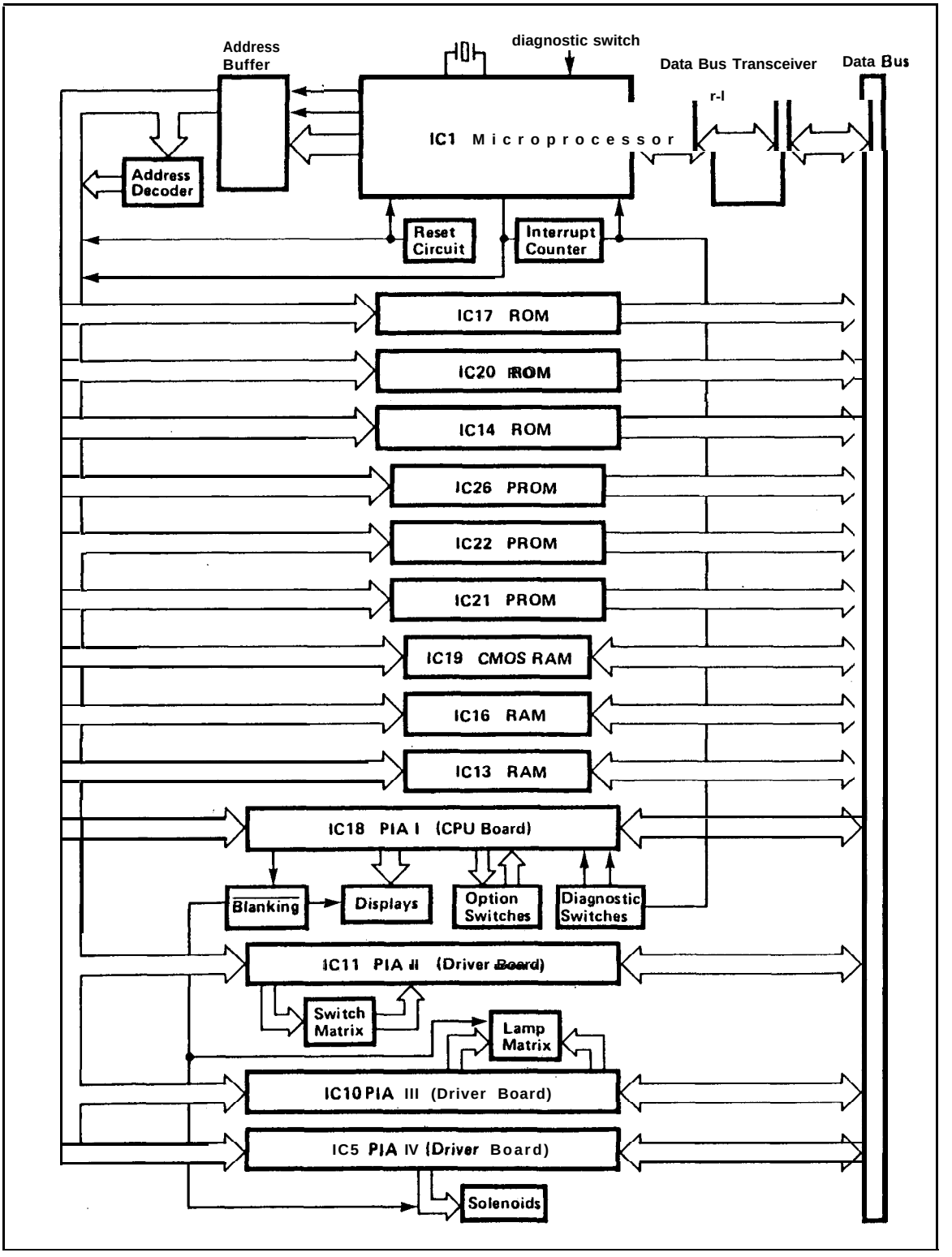
3.. CPU BOARD

Page 3-l 1 shows the general architecture of the new Williams microcomputer. Most of it is on the CPU board but the last three sets of I/O chips, called PIAs, are located on the driver board. Because of the number of parts on the bus, bus drivers and bus transceivers are utilized to help drive the bus lines to the proper threshold levels quickly and cleanly.

The CPU board underwent a major revision affecting four main areas in 1979. These are the type of microprocessor used, a redesign of the reset circuitry, a redesign of the interrupt generator, and improvements in the CMOS RAM memory protection circuitry.

Power

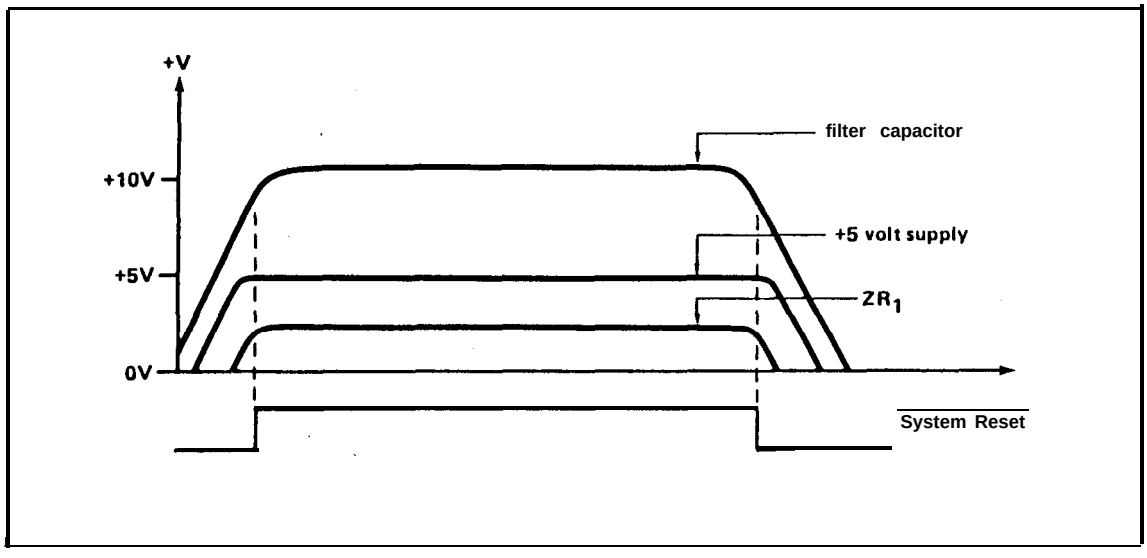
Connector 1 J2, on the upper left hand side of the CPU board, provides the unregulated t12 volts of the +5 volt regulator over one wire, and t5 volt supply and return over three pairs of wires. The +5V is the logic supply and the unregulated +12V (labelled +9V


Address Buffer
diagnostic switch
Data Bus Transceiver
Data Bus
IC1 Microprocessor
Address Decoder
Reset Circuit
Interrupt Counter
IC17 ROM
IC20 ROM
IC14 ROM
IC26 PROM
IC22 PROM
IC21 PROM
IC19 CMOS RAM
IC16 RAM
IC13 RAM
IC18 PIA I (CPU Board)
Blanking
Displays
Option Switches
Diagnostic Switches
IC11 PIA II (Driver Board)
Switch Matrix
Lamp Matrix
IC10 PIA III (Driver Board)
IC5 PIA IV (Driver Board)
Solenoids

in some Williams schematics) is used by the reset circuits to detect power-up and power-down. Test points TP9, TP10, and TP1, on the new boards, allow quick access to +5V, ground, and +12V respectively.

Reset Circuits

The reset circuit disables the CMOS bookkeeping RAM during power-down, provides a reset signal to the microprocessor at power-up, and also resets the I/O ports to the high impedance state when power is off.



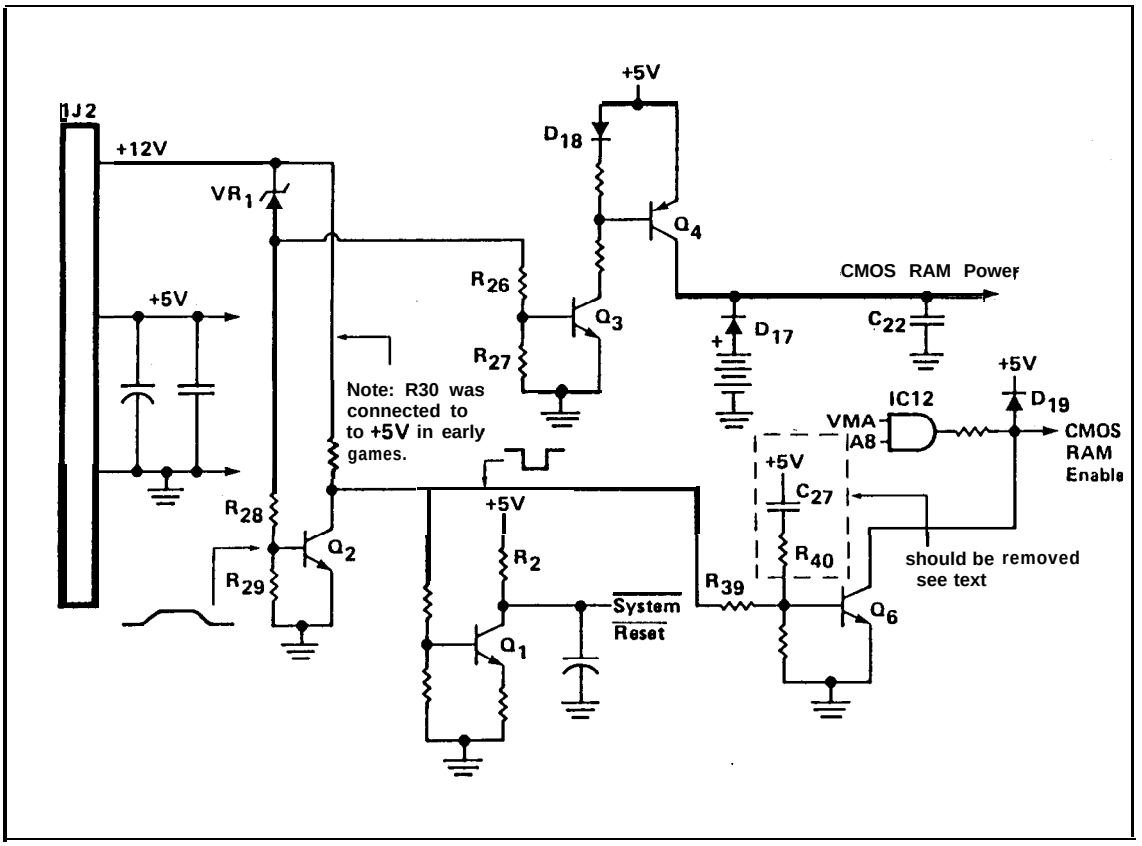
Reset Circuit — Old Board

The old reset circuit involved four smaller circuit areas. The first one detected a valid power condition. The t5 volt regulator requires +7V or more on its input to produce a clean +5.0 volt output. ZR1 is a 1 N5996B Zener diode rated at 6.8 volts and monitors the five volt regulator capacitor. When the capacitor voltage increases past 6.8 volts, a voltage appears across R29 and R27. Q2 and Q3 are switched ON at about 7.3V, by which time the logic regulator is outputting a good +5.0 volts. When power is lost, Q2, Q3 and Q6 switch OFF before the +5.0 volt logic supply is lost.

When Q3 is ON, Q4 is turned ON and the CMOS RAM is then powered by the +5V logic supply rather than the batteries. Ordinary 1.5 volt alkaline cells are used and should be replaced once a year. Diode D17 prevents damage to the batteries when game power is ON. Diode D18 prevents the batteries from discharging through the base collector junction of Q4 when logic power is OFF.

When Q2 is ON, both Q1 and Q6 are turned OFF. R2 then pulls the $\overline{\text{System Reset}}$ line HIGH, signalling IC5 to pull its $\overline{\text{Reset}}$ line HIGH, starting the MPU and PIAs. Cl is a 22μF tantalum capacitor which, together with R2, delays the $\overline{\text{System Reset}}$ signal for half a second at power-up. Q6 controls the CE2 of the CMOS RAM, IC9. When Q6 is ON -at power-up and power-down- it keeps the RAM disabled.

When game power is OFF, diode D19 clamps pin 17 of the CMOS RAM to the +5V supply which is, of course, 0 volts when power is OFF, keeping the RAM disabled.



In some of the earlier games, C27 and R40 were used. If bookkeeping memory keeps being lost on those games, these two parts should be' removed. R30 should be changed to 1 Ok instead of 1 k and be connected to the +12V supply.

Reset Circuit — New Board

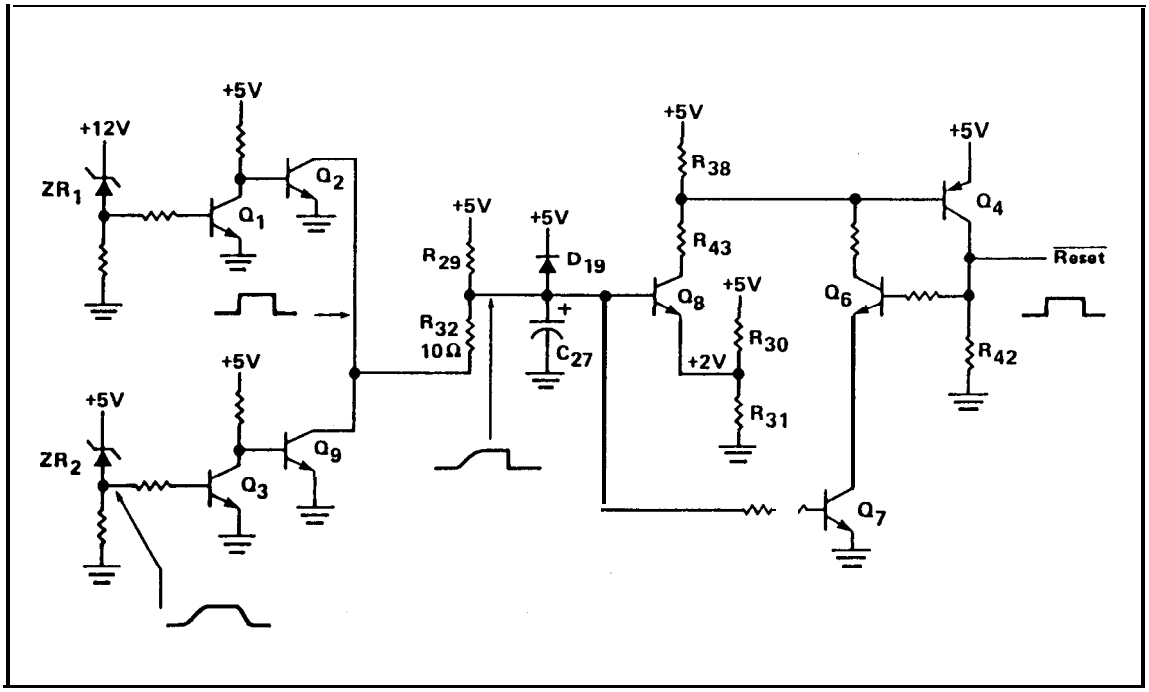
The redesign of the reset circuitry came about partially to cure past weaknesses in the older circuit and partially to rearrange it for use with the new microprocessors.

There are two valid power detection circuits. ZR1, Q1 and Q2 monitor the logic regulator filter capacitor in a similar way to the old circuit. When the capacitor's voltage surpasses 7.4 volts (approximately), Q1 turns ON, turning Q2 OFF, allowing tantalum capacitor C27 to charge via R29. ZR2, Q3 and Q9 act similarly but monitor the +5V logic supply on the CPU itself. Now, if either the filter capacitor voltage or +5V on the board is lost, C27 is immediately discharged via R32. Diode D19 clamps C27's voltage to the declining voltage of the +5V supply line and offers additional control in the event of power loss by discharging C27.

Resistors R30 and R31 keep Q8's emitter voltage at 2V. Before Q8 can turn ON, its

base must therefore be at +2.6V. This occurs about 1/10 second after power-up, as C27 charges. When Q8 turns ON, Q4's base is pulled LOW to +4.4V, turning Q4 ON. A voltage now appears across R42 and the $\overline{\text{Reset}}$ line begins to pull HIGH. Before this point, the voltage on C27 has reached a high enough level to switch Q7 ON, pulling Q6's emitter LOW. As the voltage on Q6's base now begins to reach 1 volt, Q6 is turned ON. This increases Q4's base current and Q4 turns fully ON.

If after this point, Q8 was turned OFF, Q6's collector current would assure enough base current to keep Q4 fully ON and $\overline{\text{Reset}}$ HIGH. $\overline{\text{Reset}}$ can only go LOW again if Q7 is switched OFF, which in turn switches OFF Q6 and Q4. This occurs if C27 becomes discharged to under 1 volt.



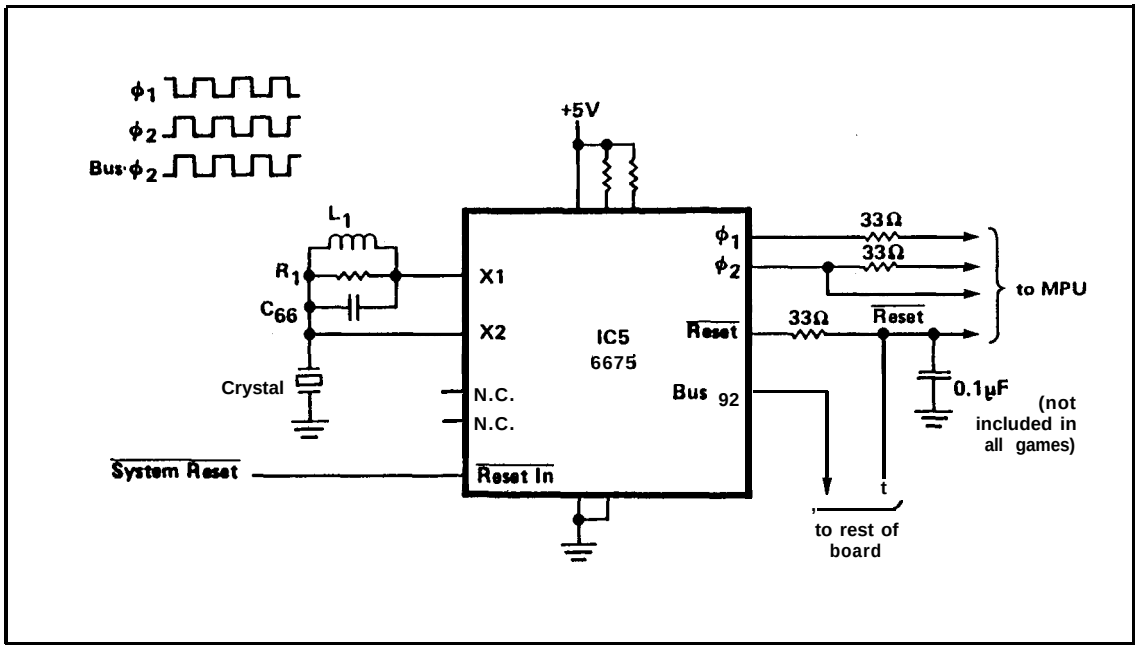
Power to the CMOS RAM is provided by the +5V logic supply through D18 and by the batteries through diode D17. D18 prevents the battery from discharging through the board when logic power is gone and D17 protects the battery when logic power is available. (Refer to diagram on page 3-24.)

$\overline{\text{Reset}}$ controls the MPU, CMOS RAM and PIAs directly in the new board.

System Clock — Old Board

The old CPU board uses a Motorola MC6875 clock chip at IC5 and a 3.58 MHz colour television crystal'to produce the 2-phase clock outputs and control the board's Reset line.

R1, L1 and C66 make up a "tank" circuit which helps stabilize the oscillator during power-up. The oscillator frequency is divided by four, internally, to about 900 kHz. $\phi 1$ and 42 are of opposite phase and drive the MPU's clock inputs. "Bus$\phi 2$" is in the same phase as $\phi 2$ but is used for timing in the rest of the microcomputer. The System $\overline{\text{Reset}}$ output from the reset circuits is input to IC5. A low impedance output buffer controls the $\overline{\text{Reset}}$ line which controls the MPU and other parts on the board.



Motorola MC6800 Microprocessor — Old Board

The Motorola MC6800 MPU is an 8 bit microprocessor with 16 address lines. The address lines often output erratic values and so, a VMA line (valid memory address) output is used by the address decoding circuit to select memory devices only when there is a valid memory address on the bus (VMA is HIGH).

The R/W line is LOW for a write and HIGH the rest of the time. The eight data lines are bidirectional and are in the high impedance state whenever DBE (data bus enable) is LOW or the R/W line is HIGH.

A new address is put out on the address bus about 200 to 300 nsec after $\phi 2$ (and Bus$\phi 2$ goes LOW. Data transfers occur three quarters of a cycle later when $\phi 2$ makes a negative transition again. (The maximum clock frequency of the 6800 is 1 MHz.)

The 6800 operates off +5 volts and has two ground connections. Two of the MPU's pins are not used in the Williams' system (Halt and TSC) and are tied HIGH and LOW

respectively. Two other pins are not connected internally in the MPU and are tied to ground.

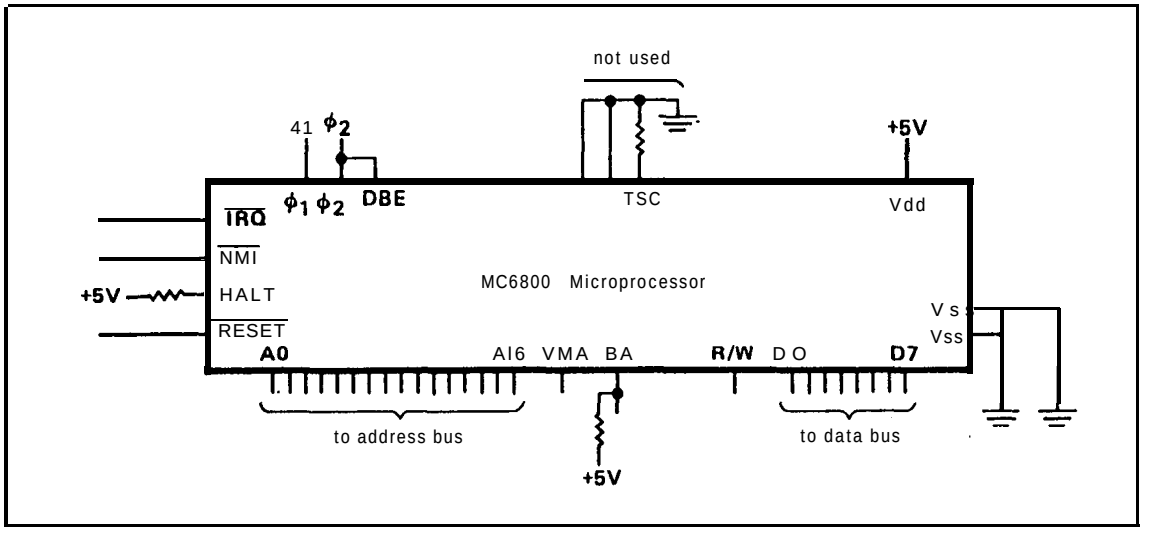
The $\overline{\text{RESET}}$ input is controlled by the clock chip, IC5. The reset circuits control the $\overline{\text{Reset}}$ output of IC5. After the +5V supply reaches about 4.75 volts, the oscillator is producing the 2-phase clock signals for the MPU, and within 8 cycles, VMA is brought LOW. This will keep the CMOS RAM disabled as Q6 of the reset circuit turns OFF. Relatively speaking, the MPU has a fair bit of time to stabilize control of VMA before $\overline{\text{Reset}}$ goes HIGH.

The 6800 can now begin execution and it does this by first going to ROM addresses FFFE and FFFF (hexadecimal) in IC17 and fetches the address of the first program instruction from these two bytes, then loads it into the MPU's program counter. The microcomputer is now ready to begin execution of the program.

The $\overline{\text{IRQ}}$ input is the interrupt request input. When this line is pulled LOW, an interrupt is signalled to the MPU. The 6800 saves internal register data in the general RAMs and then looks up the beginning address of the interrupt program in locations FFF8 and FFF9. At the end of the interrupt sub-program, the MPU retrieves the stored register data from the RAM and resumes execution of the program it was previously executing.

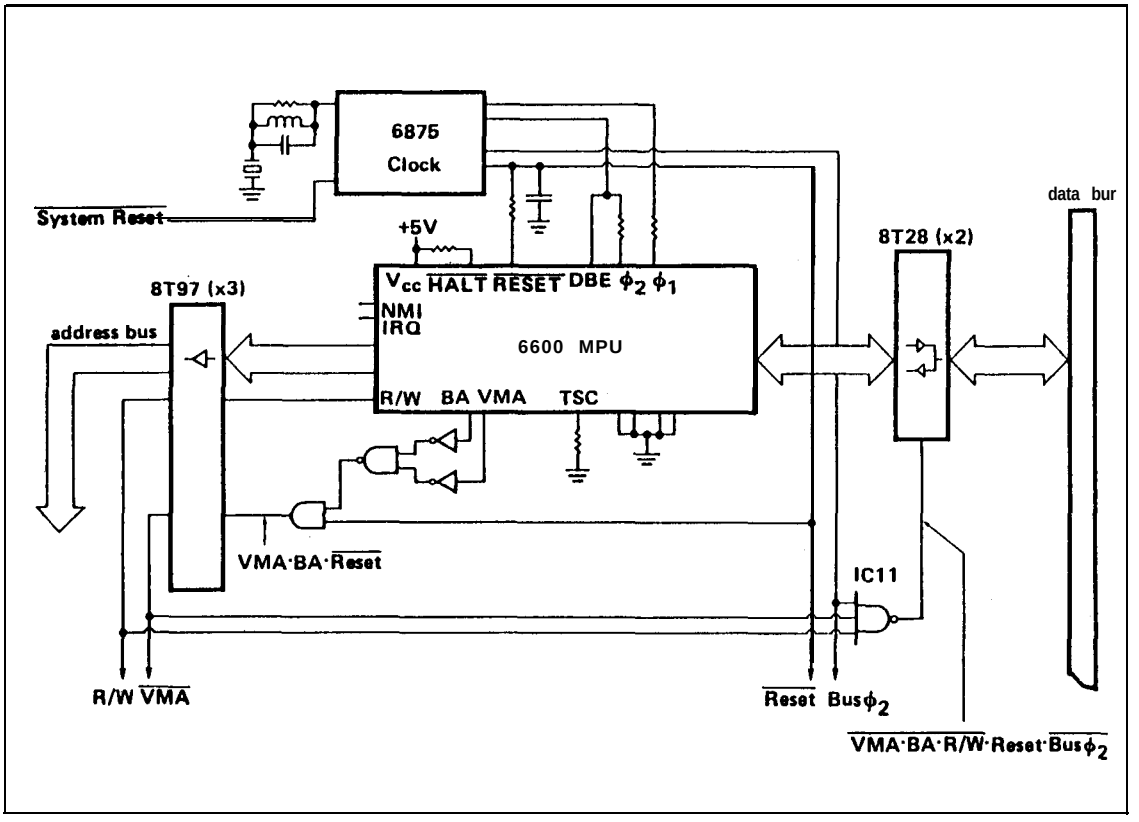
The $\overline{\text{NMI}}$ input is a second interrupt input called the non-maskabie interrupt, which means that this input cannot be disabled by the program. Action taken is similar to that for the $\overline{\text{IRQ}}$, except that the sub-program address is stored in locations FFFC and FFFD.

The $\overline{\text{HALT}}$ input of the MPU can be used to stop the MPU from executing instructions by being pulled LOW. This puts all the bus lines in the high impedance state (including R/W) but leaves VMA LOW. BA (busavailable) will be HIGH, indicating that the MPU is not using the busses. There is also a program instruction which can put the MPU in a "wait state". This is similar to a $\overline{\text{HALT}}$, except that the MPU will start up again after an interrupt,



Bus Control — Old Board

The diagram below shows how the 6875 clock chip and 6800 MPU connect together. The clock starts oscillating as power comes on in the board and moments after, the reset circuitry pulls System Reset HIGH. The Reset output of the 6875 then goes HIGH, starting the MPU. When power is about to be lost, System Reset and Reset are pulled LOW, stopping the MPU and turning the rest of the microcomputer OFF before loss of +5 volt power. Busϕ2 is available for the rest of the system.



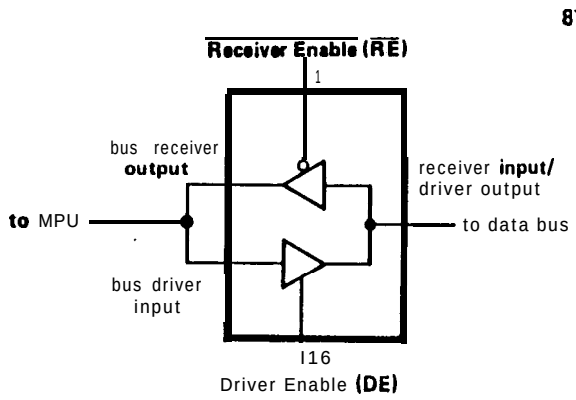
Three 8T97 hex buffers are used to drive the 16 address lines and VMA and R/W lines. Note that VMA is really VMA·BA·$\overline{\text{Reset}}$. The inputs of the 8T97 are high impedance. The outputs can source 5mA and sink 48mA, which is far greater than the 6800's output capabilities.

The data bus is buffered similarly to the address bus, except that two bidirectional 8T28 bus transceivers are used. These have back to back buffers called receivers and drivers.

Both the inputs are high impedance. The receiver output can source 2mA and sink 20mA and is connected to the MPU and driver input outside the chip. The driver output can source 10mA and sink 48mA, and drives the bus.

The receiver enable is activated when LOW and driver enable is activated when HIGH. Both of these enables are tied together so that data can only travel in one direc-

tion at a time. These inputs are controlled by IC11 pin 12. This is actually the signal $\overline{VMA \cdot BA \cdot R/W \cdot Bus \cdot \phi 2 \cdot RESET}$. When this signal is LOW, data is transferred from the data bus to the MPU, and when HIGH, it is written from the MPU to external devices.



The bus drivers are required to drive all the parts on the bus on both the CPU board and driver board. Without them, at this high a clock frequency, the processor could not drive the voltage levels on the bus lines properly LOW and HIGH quickly enough.

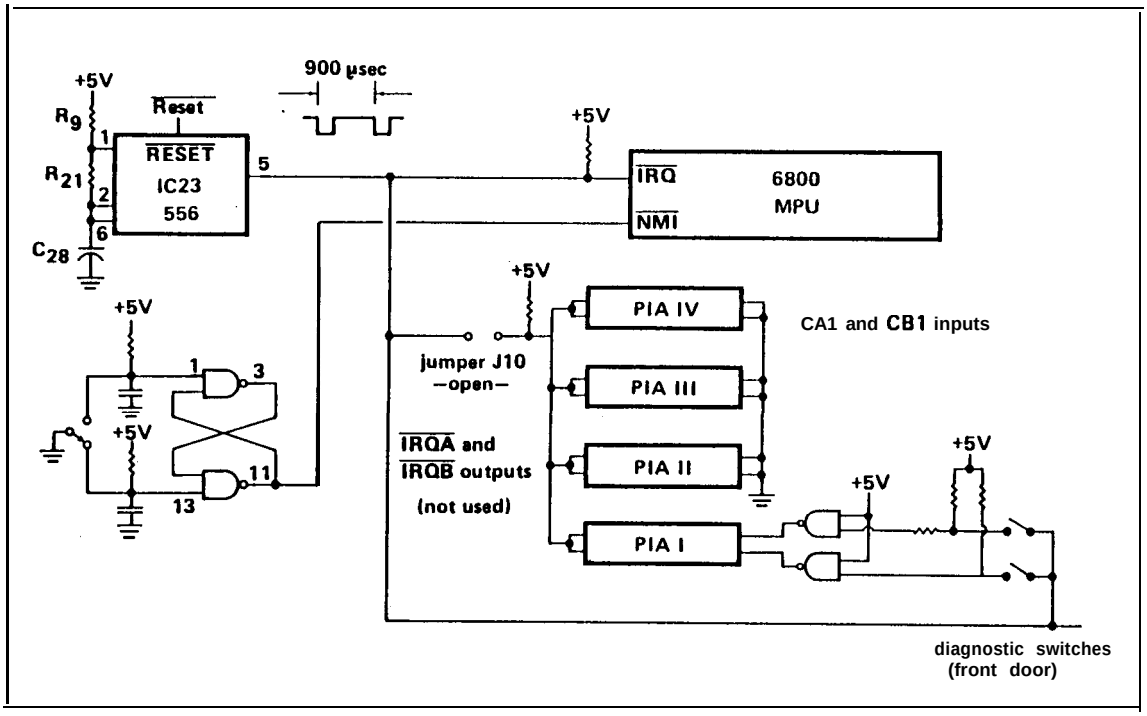
Interrupt Control of the System – Old Board

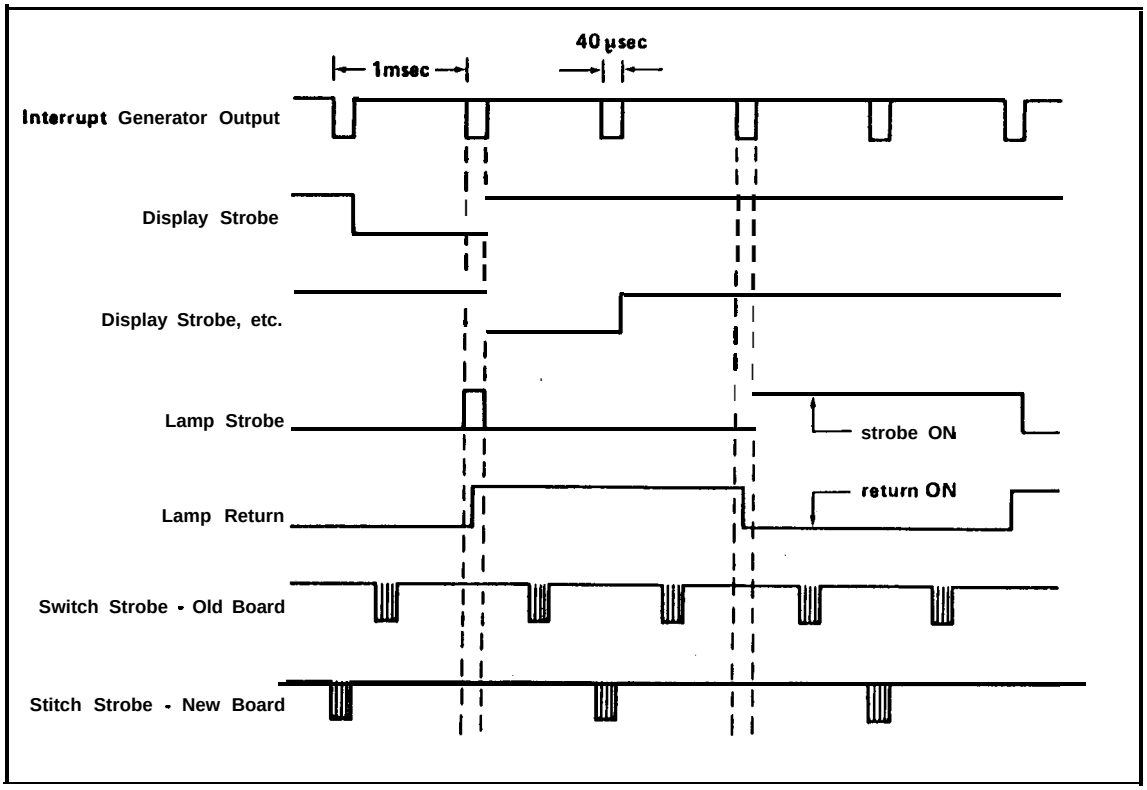
The $\overline{NMI}$ input of the MC6800 is used to start the diagnostic program for the self-tests and game status changes. These functions are discussed in detail in each game's operator's manual from Williams.

Switch Swl is located on the lower right of the CPU board below the "enter" switch. The NMI input is buffered by an SR flip-flop made out of two gates in IC24. These act as a switch debouncer. Pin 11 is HIGH when pin 13 is held LOW. Pin 11 will go LOW, causing an interrupt, if both pin 13 goes HIGH and pin 1 is held LOW. Pin 11 will go HIGH again only when pin 13 is pulled LOW again.

The IRQ input is used as a time interval counter. It is used to control the length of time that a coil is turned ON, to sequence the display and lamp strobes and strobe the diagnostic switch inputs. The source of the interrupts is the interrupt generator, below, in 1/2 of IC23. This is a 556 timer chip which is the equivalent of two 555 timers in the same package. R9 and R21 charge C28 up to 2/3 of +5V, at which point pin 2 turns ON the discharge pin, pin 1, which discharges C28 through R21. When C28's voltage reaches 1/3 of +5 volts, pin 6 turns pin 1 OFF again, allowing C28 to charge again. Output pin 5 is LOW when C28 is discharging.

The $\overline{Reset}$ output of the 6875 controls the reset input of this circuit, keeping C28 discharged and the output LOW when $\overline{Reset}$ is LOW.


+5V
R9
Reset
900 µsec
+5V
R21
RESET
IC23
556
C28
IRQ
NMI
6800
MPU
+5V
+5V
PIA IV
CA1 and CB1 inputs
jumper J10
–open–
PIA III
IRQA and
IRQB outputs
(not used)
PIA II
+5V
+5V
PIA I
diagnostic switches
(front door)


40 µsec
1msec
Interrupt Generator Output
Display Strobe
Display Strobe, etc.
Lamp Strobe
strobe ON
Lamp Return
return ON
Switch Strobe - Old Board
Stitch Strobe - New Board

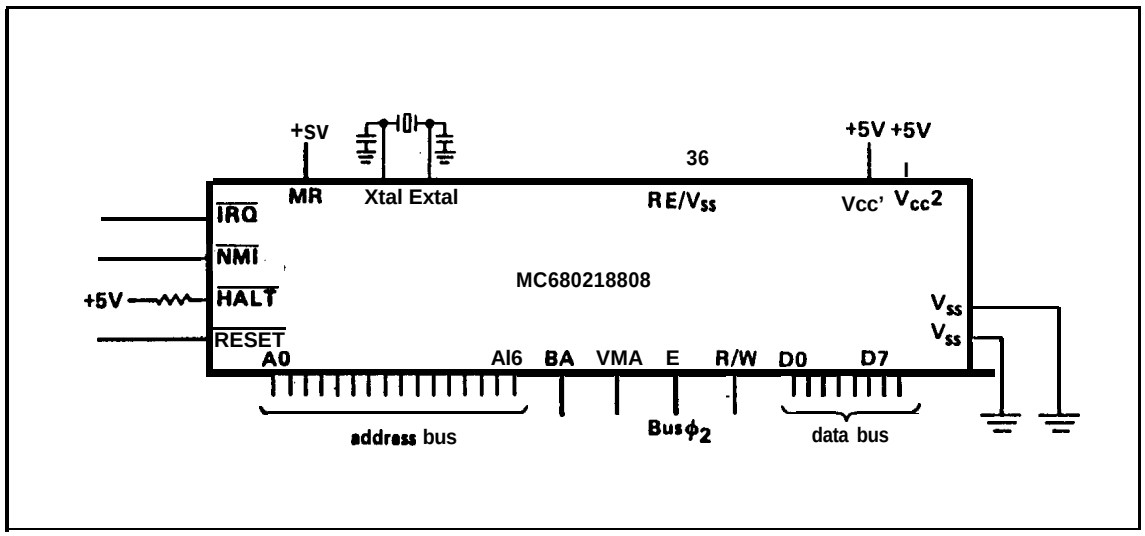
The interrupt generator runs at a frequency of about 1,100 Hz and the output signal has a period of about 900 μ sec.

Note in the facing diagram that the PIAs (described on page 3-26) do not interrupt the MPU. Instead, PIA I is checked by the main program automatically through the data bus and internal registers of the PIA. The CA1 and CB1 interrupt inputs are used then, as input switch latches for the front door diagnostic switches.

Motorola MC6802/MC6808 Microprocessor — New Board

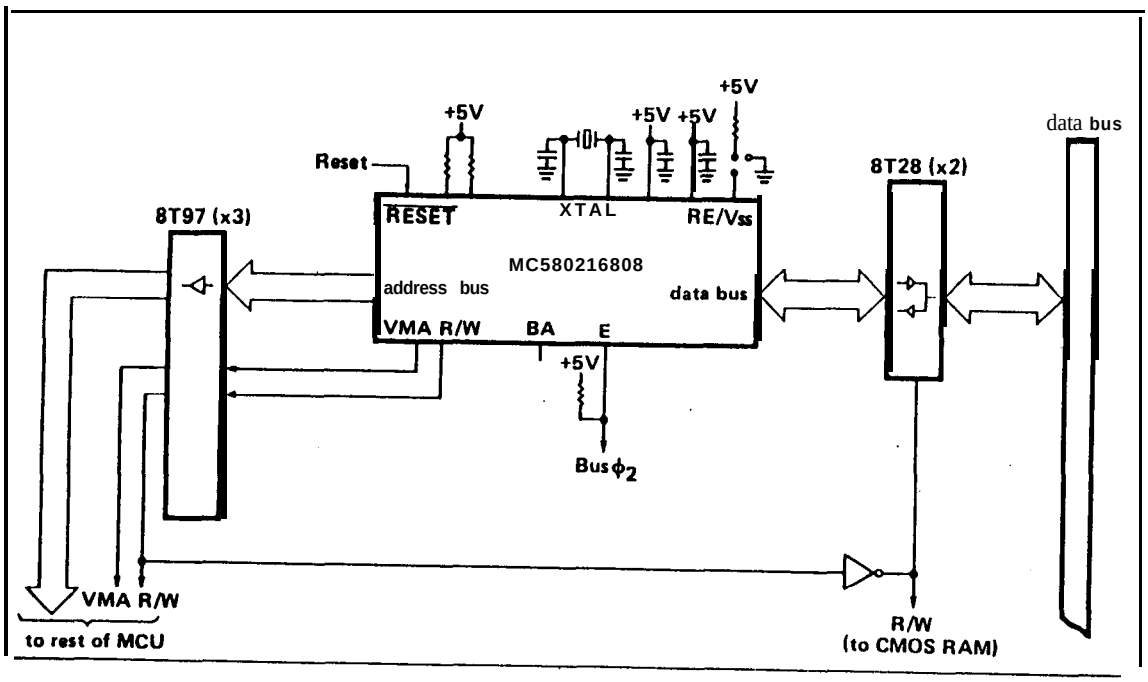
The MC6802 and MC6808 microprocessors are both similar to the MC6800 microprocessor but share some important differences. Both have their own built-in clock circuit. The crystal is attached to two pins of the MPU and two 27pF capacitors are used for oscillator stability. The Bus ϕ2 signal is now an output of the MPU and this pin is usually called "E" or "Enable" by Motorola. The DBE input is permanently connected internally in the MPU and so there is no pin. There is no TSC pin either. The MR pin is for special applications and is tied HIGH in the Williams boards.

The MC6802 also has its own built-in 128 word by 8 bit RAM. One of the two Vcc pins in the 6802 is for powering a portion of this RAM. Pin 36 is the "RE" input (RAM Enable). When HIGH, the internal RAM responds to the hexadecimal addresses 0000 to 007F. Pin 36 of the MC6808 is a Vss pin and must be connected to ground. When an MC6802 is used in the new board with RE pulling HIGH, the MC6810 RAM at IC13 is not used.

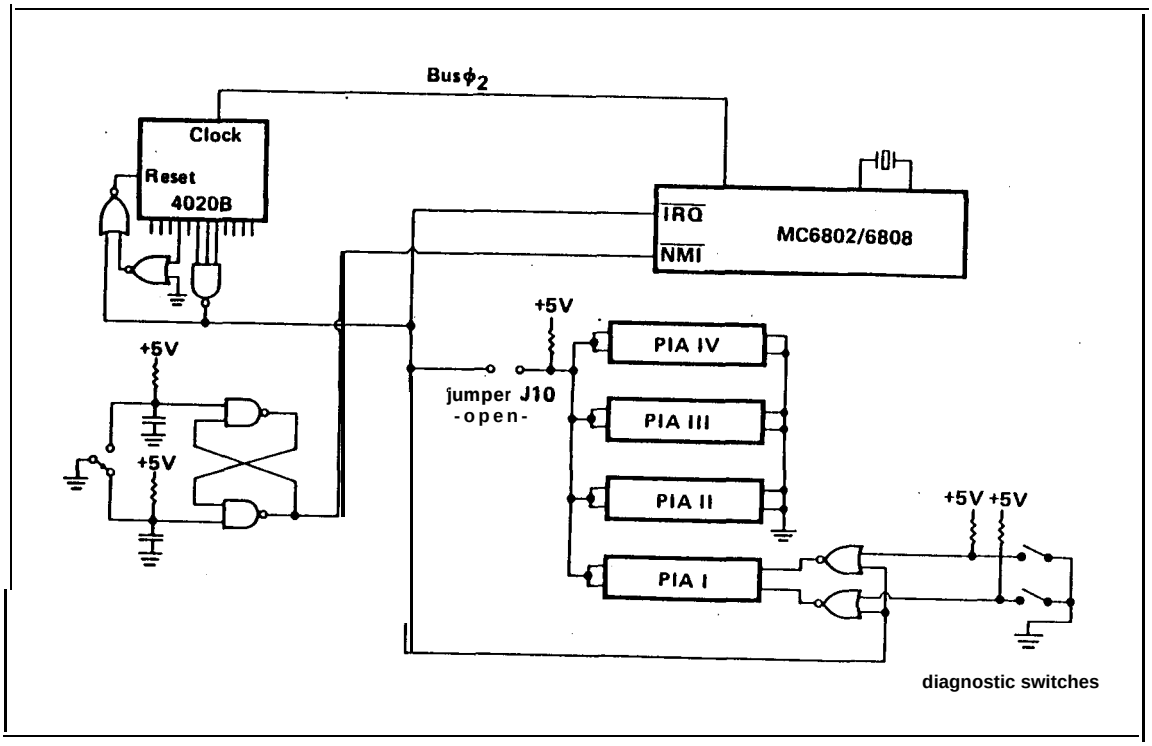


Bus Control — New Board

The new CPU board has a simpler bus control system. Three 8T97 buffers are still used to buffer the sixteen address lines, R/W, and VMA. Note that VMA is not gated with any other signal in the new board. The R/W line controls the two 8T28 bus transceivers through a 7404 inverter. The output of this inverter also controls the OD (output disable) pin of the CMOS RAM. One Reset line is shared by the whole microcomputer and controls the MPU directly.



Interrupt Control of the System — New Board



The $\overline{NMI}$ input of the MC6802/MC6808 MPU is still used to start the diagnostic program. The interrupt generator circuit, though, has been replaced by an interrupt counter circuit. The 3.58 MHz crystal frequency is divided by 4 in the MC6802/MC6808 to about 900 kHz and is output as Busϕ2. This signal is counted down by a 40208 CMOS counter. This chip has 14 counting stages with a clock input and reset input. Only 12 bits are output, though.

The 128s, 256s, and 512s outputs go HIGH after the first 896 count cycles (approx. 1 msec). The output of a 74LS103-input NAND gate goes LOW at this point, pulling the $\overline{IRQ}$ input of the MPU LOW. 36 μsec later, the 32s output goes HIGH and is inverted by a 74LS02 NOR gate. The output of this chip and the LS10 are input to a second LS02 NOR gate whose output raises the Reset pin of the 40208 HIGH. This resets all the counter output pins LOW and the counter commences counting again from zero.

The program counts $\overline{IRQ}$ interrupts as being 1 msec long. The older circuit was usually close to producing an interrupt pulse every 900 μsec approximately. With crystal control, the new counter produces a signal every 1036 μsec and is constant from game to game.

The reading of the diagnostic switches is identical to the old method; however LS02 NOR gates are used instead and the $\overline{IRQ}$ signal is not gated through the switches.

Memory Map

The following chart indicates the addresses required on the bus lines in order to select each of the thirteen devices on the bus. Note that PIAs II, III and IV are located on the driver board. RAM1 can either be in a MC6802 at IC1 or in position IC13. For all devices, VMA and Busϕ2 must be HIGH. The RAMs are at the lowest addresses, the ROMs are at the highest addresses. The ROMs are 2K x 8 and the PROMs are 512 x 8. The ROM at IC14 is not used if PROMs are used. (Note similar address codes for AI 1 and A12.) Also, the PROM at IC26 was not used in games before "Phoenix". "x" indicates that this address line is used for internal memory location addressing. A blank indicates no connection. The address decoding circuits are fairly simple and discussed with each of the parts.

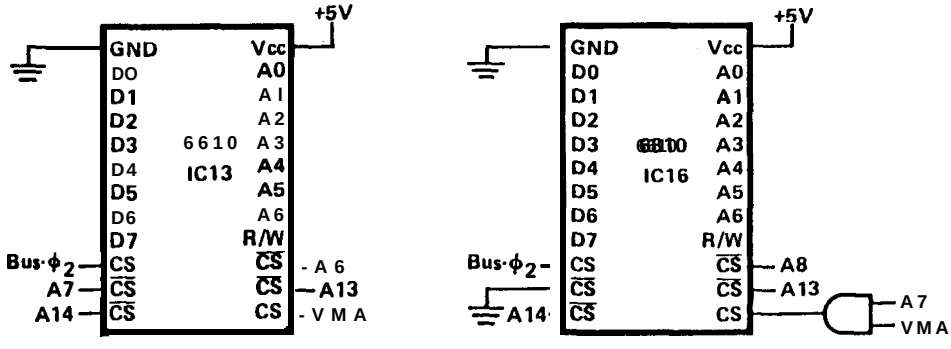
DEVICE	VMA	BUS·ϕ_2	AI4	AI3	AI2	AII	A10	A9	AB	A7	A6	A5	A4	A3	A2	AI	A0
RAM 1	1	1	0	0					o	o	x	x	x	x	x	x	x
RAM 2	1	1	0	0					0	1	x	x	x	x	x	x	x
CMOS RAM	1	1		0					I	x	x	x	x	x	x	x	x
PIA 1	1	1	0	1		1										x	x
PIA 2	1	1	0	1	1											x	x
PIA 3	1	1	0	1			1									x	x
PIA 4	1	1	0	1				1								x	x
PROM IC21	1	1	1	1	0	0	0	0	x	x	x	x	x	x	x	x	x
PROM IC22	1	1	1	1	0	0	0	1	x	x	x	x	x	x	x	x	x
PROM IC26	1	1	1	1	0	0	1	0	x	x	x	x	x	x	x	x	x
ROM IC14	1	1	1	1	0	0	x	x	x	x	x	x	x	x	x	x	x
IC14 (in new board only)			1	1	0	1	x	x	x	x	x	x	x	x	x	x	x
ROM IC20	1	1	1	1	1	0	x	x	x	x	x	x	x	x	x	x	x
ROM IC17	1	1	1	1	1	1	x	x	x	x	x	x	x	x	x	x	x

RAM

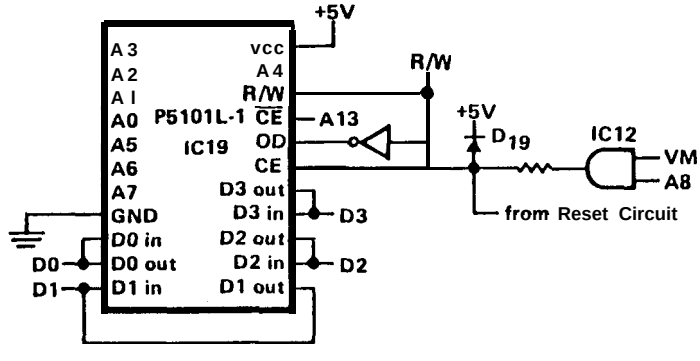
There are three RAMs used in the Williams systems. IC13 and IC16 are Motorola M6810 128 x 8 NMOS RAMs. They have six chip selects each and bidirectional data lines. If the RAM in an MC6802 is used at IC1 in the new board, then IC13 is not needed. IC13 and IC16 are connected the same way in both the early and new boards.

The third RAM is an Intel P5101 L-I CMOS RAM (or equivalent) with a memory capacity of 256 words by 4 bits. The slower speed versions of this part will not work in these boards. It is battery backed-up and used as bookkeeping memory. The 5101 has four data input lines and four data output lines, The output disable (OD) pin disables the output pins when HIGH. In the old board, the R/W line was inverted by a 7404 inverter to control OD. During a write, the R/W line went LOW and OD went HIGH.

The reset circuit pulled CE2 LOW during power-up and power-down. Diode D19 clamped this pin to the t5 volt line when. power was OFF, keeping it LOW. In normal power-up conditions, IC12 ANDed VMA and A8 as part of the address decoding circuit.

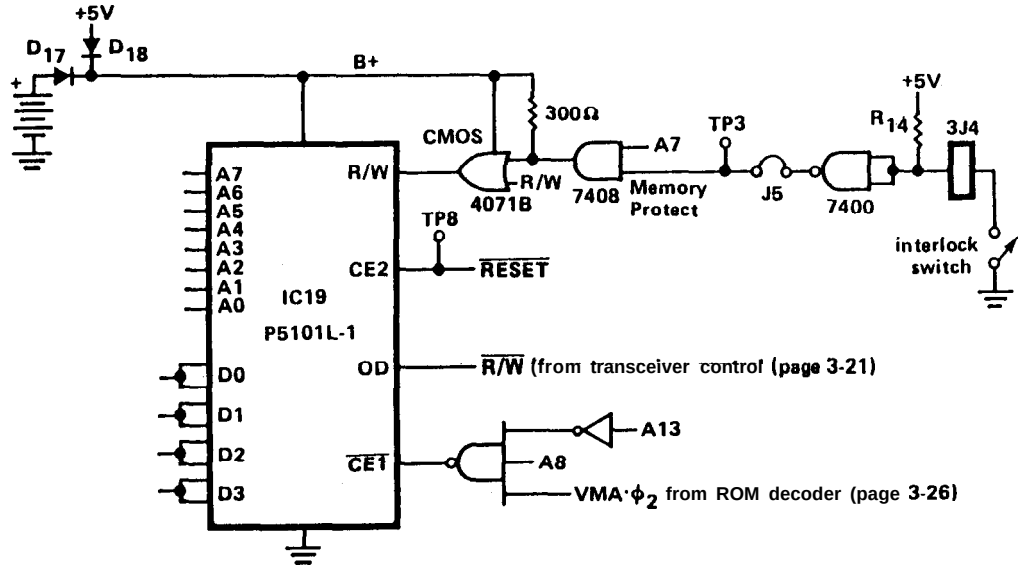


NMOS RAMs - Both Board



CMOS RAM - Old Board

In the new board, the 7404 controlling the data bus transceivers controls the OD pin. The Reset circuit controls CE2. Address lines A13, A8 and VMA and $\phi 2$ control $\overline{CE1}$ during normal power-up operation. A 4071B CMOS OR gate controls the R/W line. In order for a write to occur, both the R/W and $\overline{CE1}$ pins must be LOW.



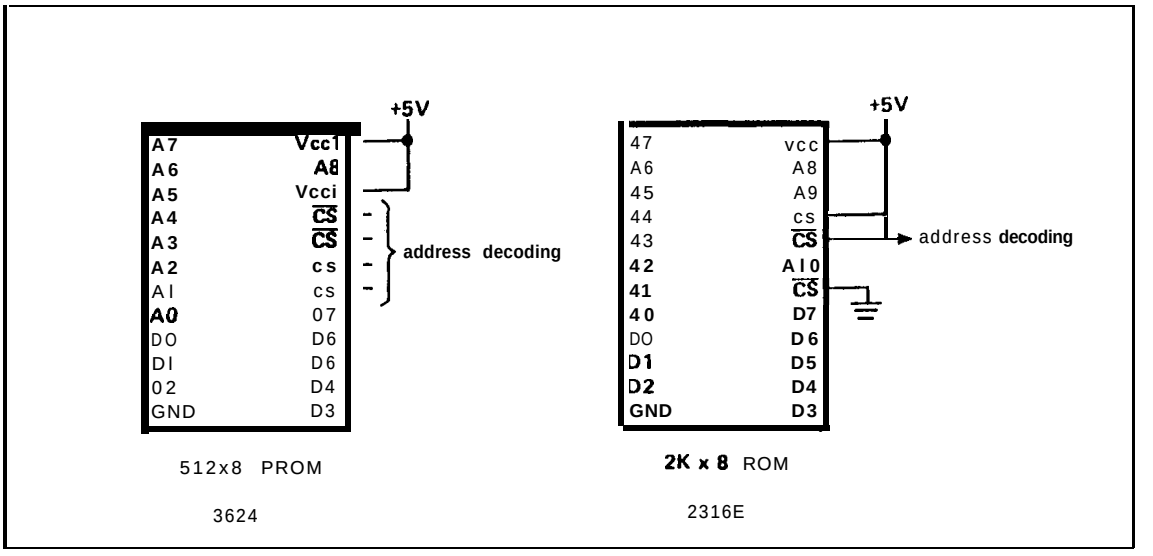
CMOS RAM - New Board

The interlock switch in the front door is opened whenever the front door is open. R14 pulls the 7400 NAND gate inputs HIGH, which causes one of the inputs of the 7408 AND gate to be pulled LOW. This causes the second input to the 40718 OR gate to be LOW and the CMOS RAM can then be written into.

On the other hand, if the front door is closed, the 7400 input is LOW, Memory Protect is HIGH and if address line A7 goes HIGH, the R/W line cannot go LOW. In this case, data cannot be overwritten into the RAM. Therefore, data can only be written into the top half of the RAM contents when the front door is open, such as when the bookkeeping data is being changed by the operator. All bookkeeping data which is not updated by the machine itself is stored in this area.

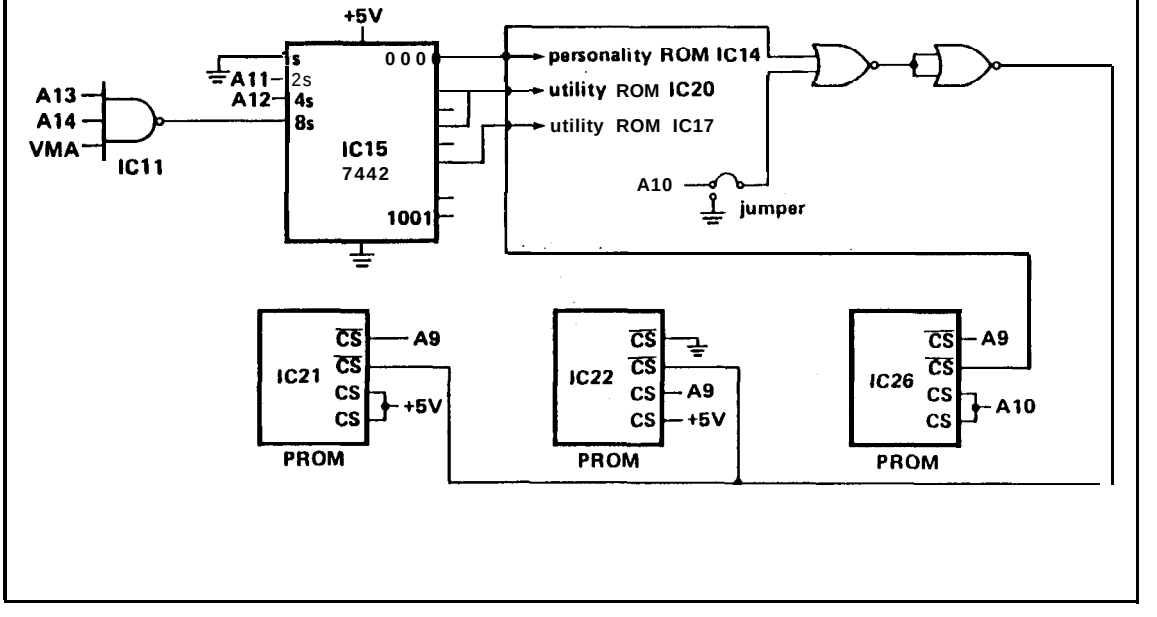
Program Memory

There are two types of program memory used in the Williams games. These are the Intel types 3624 512 x 8 bipolar PROMs and 2316E 2048 x 8 MOS ROMs. Locations IC21, IC22 and IC26 are used for PROMs only. Locations IC14, IC20 and IC17 are reserved for ROMs only. In most games, IC17 and IC20 are standard utility ROMs. A personality ROM may be used at IC14. Most often,though, personality PROMs will be used which share the same memory map locations as IC14 (refer to the address map on page 3-22). IC26 is not found on games made before "Phoenix".

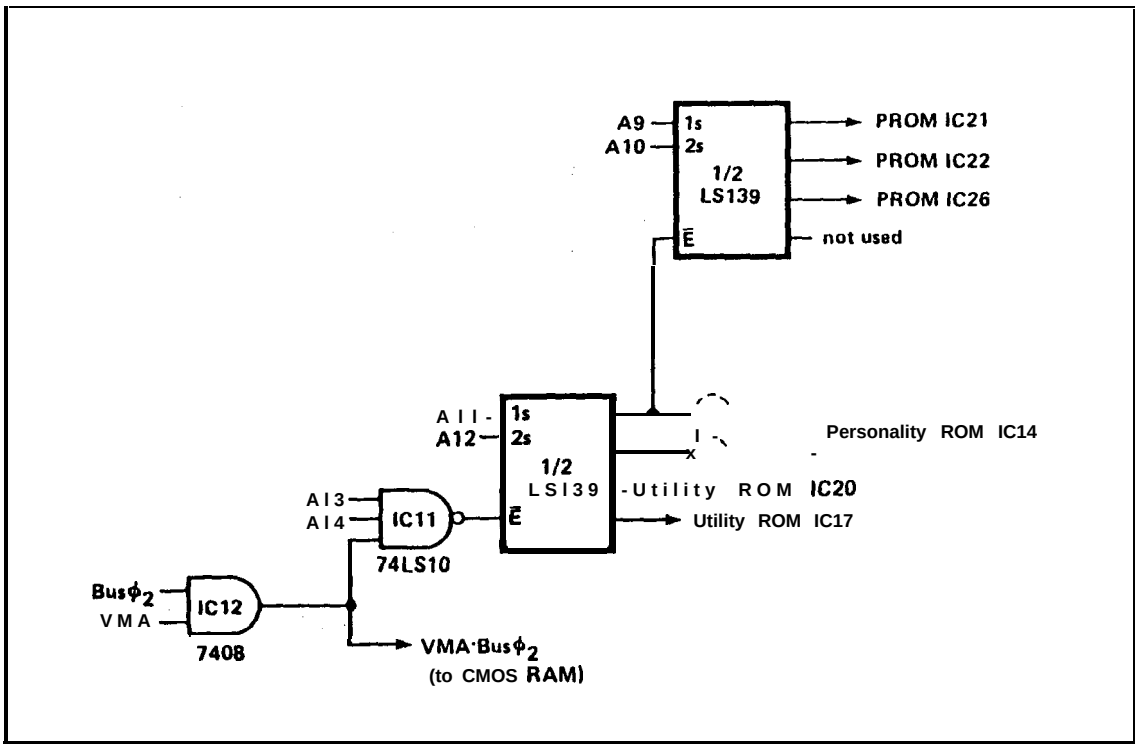


Program memory address decoding in the old CPU board is accomplished with three gates and an MSI decoder in two stages. First, part IC11, together with IC15, a BCD to decimal decoder, decode for the two utility ROMs and personality ROM/PROMs. Additional lines on the PROM chip selects further decode address lines A9 and A10. Note that only one output at a time is pulled LOW in the 7442, depending upon the BCD input **code.**

In the new CPU board, two gates and both halves of a 74LS139 dual binary to one of four decoder are used. **A 7408 AND gate provides a VMA·ϕ2 signal which is also used in the new CMOS RAM circuit. A 74LS10 3-input NAND gate enables the first decoder**



when program memory is to be accessed. The two utility ROMs at IC17 and IC20 are both enabled directly by the decoder. If a personality ROM at IC14 is used, it can be jumpered for one of two addresses (A1 1 HIGH or LOW). Addresses for personality PROMs are decoded further by the other half of the LS139.



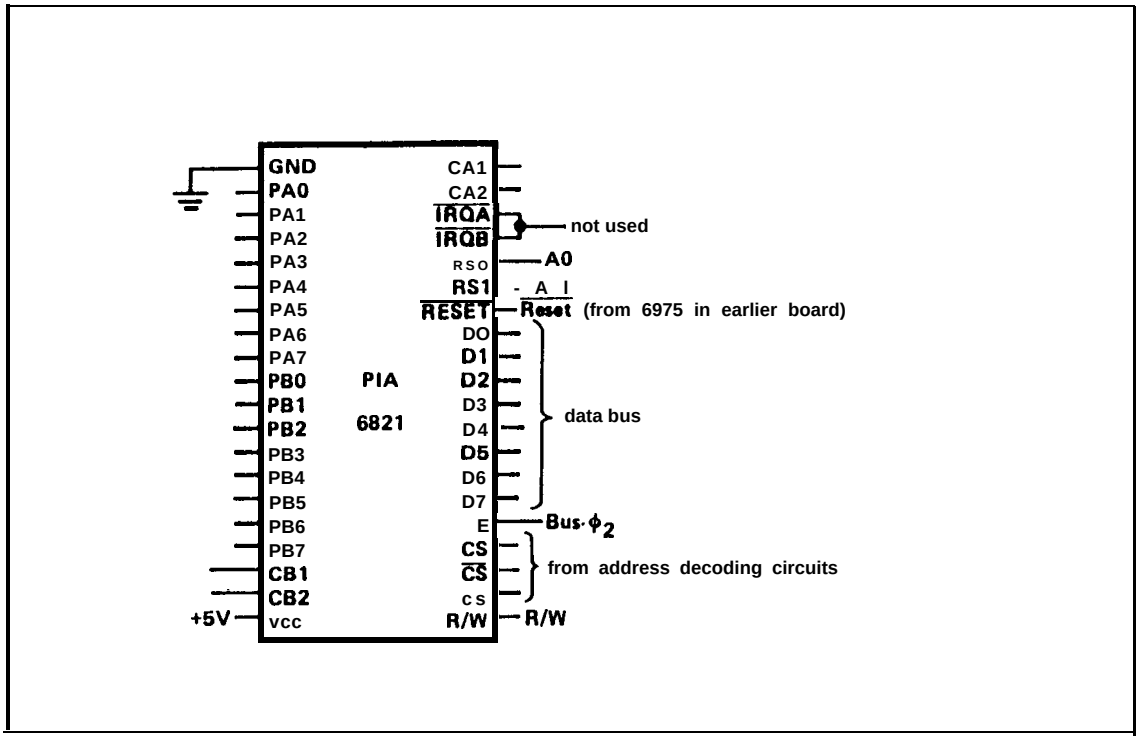
Peripheral Interface Adapter (PIA) — Input/Output (I/O) Chips

Motorola call their MC6820 (now discontinued) and MC6821 peripheral interface adapters or PIAs for short. They have three sets of I/O ports. The first consists of the eight lines PA0 through PA7 and CA2. They are bidirectional ports with an open drain output and internal pull-up resistors. As an input, each port is equivalent to one TTL load.

The second set of ports are the lines PB0 through PB7 and CB2. As inputs, they are in the high impedance state, and as outputs, like the first set of ports, they can drive one standard TTL input. However, they have a high current sourcing ability of greater than 1mA.

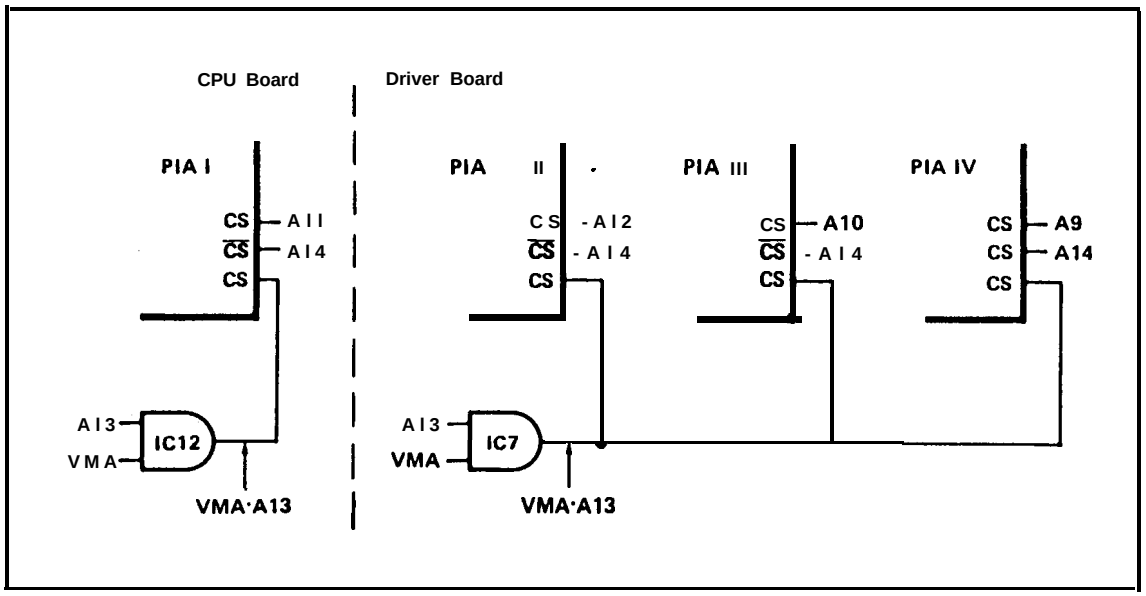
Any of these lines can be programmed individually by the microprocessor as either inputs or outputs by setting certain internal registers within the PIA. When the CA2 or CB2 lines are programmed as inputs, however, they activate the IRQA or IRQB outputs respectively. In the Williams game, though, they are used as outputs only.

The last set of ports are the CA1 and CB1 lines. These are inputs only and cause the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ outputs to go LOW when activated. The microprocessor can program either of the two inputs to become activated with either a positive or negative input transition. Only CA1 and CB1 of PIA I are used in this system, however, and the $\overline{\text{IRQA}}$



and $\overline{IRQB}$ outputs do not connect to the MPU (see Interrupt Control of the system, pages 3-18 and 3-21).

On the microcomputer side of things, the PIA is selected by means of three chip selects which are connected to VMA, Al 4, Al 3, plus one other address line. The following diagram illustrates the connections.



Busϕ2 connects to the enable input. Data transfers occur over the data lines and the direction is controlled by R/W. The register selects select the internal registers. The $\overline{\text{Reset}}$ input is controlled by the $\overline{\text{Reset}}$ line and initializes the chips at power-up. When $\overline{\text{Reset}}$ is LOW, all the ports are in the input mode.

PIA I Port Circuits

PIA I, located on the CPU board at IC18, is responsible for outputting the system display digit strobes and both sets of BCD data to the master driver board. It also reads the data and function switches, controls the two self-test LEDs, and inputs the diagnostic switch inputs from the front door. Please refer to page 3-30 for the following discussion.

Lines PBO through PB7 control the BCD1 and BCD2 outputs for the displays. Lines PA0 through PA3 control a 74154 TTL binary to one of sixteen decoder, IC6. Each of sixteen output lines is specified by a four bit number presented to the input pins. When an output is specified, it goes LOW. Only one output can be specified at a time. In operation, the 74154 strobes one digit strobe line after another non-stop on a continual basis.

All the outputs for the displays are static protected with 470pF capacitors and 1 k resistors. These outputs all drive CMOS inputs on the master display board, so the 4.7k resistors are required to pull the HIGH levels HIGH enough to meet the input HIGH thresholds of the parts on the master display driver board.

Outputs 0000 through 0011 (binary), of the decoder, strobe, with LOW strobe pulses, the four groups of switches that make up the data and function switches. These switches are in a matrix, so diodes are required in series with each switch. The pull-up resistors maintain the return lines HIGH when the switches are open. The returns are connected to the driver inputs of an 8T28 data bus transceiver at IC2 (the same type used to drive the data bus).

Unless the game is in the diagnostic mode, the CA2 output is HIGH and the output at pin 6 of the 7404 inverter at IC7 is LOW, enabling the $\overline{\text{RE}}$ (Receiver Enable) input of IC2. In this m&the PA4 and PA5 outputs of PIAI control the two LEDs. When SW1 is pressed, the NMI interrupt input of the MPU is activated and the board performs a self check on itself. After this, the game is in the diagnostic mode, CA2 is LOW and $\overline{\text{RE}}$ is HIGH. PA4 through PA7 are in the input mode. If SW2, the "Enter" switch is pressed, DE (Driver Enable) goes HIGH and the option switch returns now control those PIA inputs. If at least one of the switches is closed, one of the ports will be strobed LOW, and the processor will know that someone is pressing the "Enter" switch.

The PA2 port of PIA I also controls the blanking circuit. The purpose of the $\overline{\text{Blank}}$ & signal is to disable solenoid, lamp, and display circuits at power-up, power-down, and in the event of a microcomputer failure.

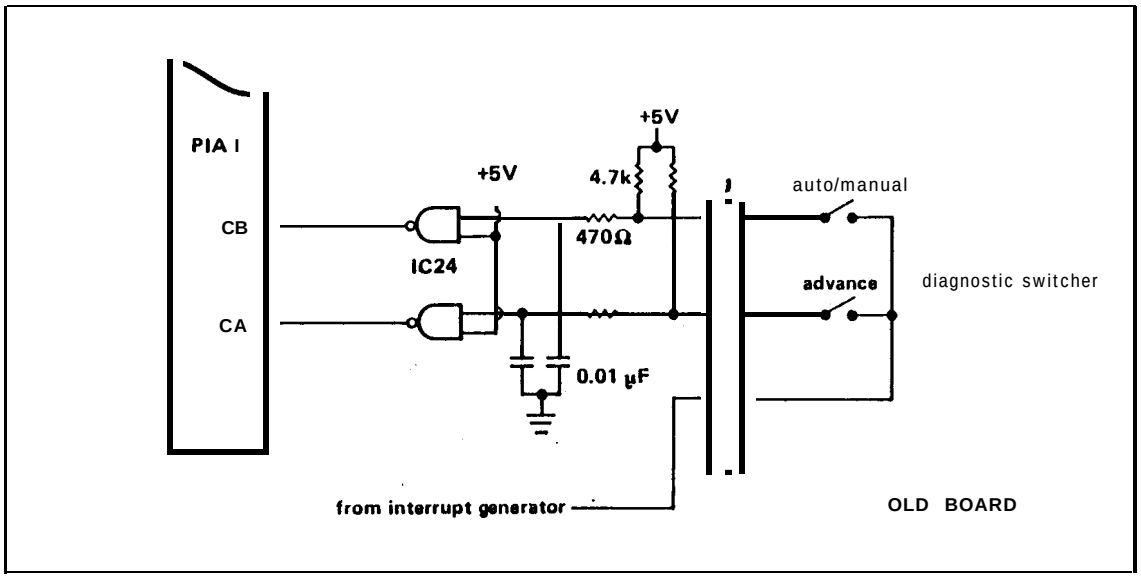
The blanking circuit is based around ½ of IC23, the 556dual timer chip. This part is equivalent to two 555 timers. In the absence of output signals from PA2, R23 pulls both the base of Q5 and the trigger input, pin 8, of IC23 HIGH. Q5 is therefore turned OFF and C31 charges, via R22. When the capacitor reaches 3.3 volts, the threshold input of IC23, pin 12, sets an internal flip-flop and both the open collector discharge output, pin 13, and the Q output, pin 9, are pulled LOW. This is the Blanking line and disables the driver circuitry when LOW.

$\overline{\text{Reset}}$, from the reset circuits, also controls the timer. When $\overline{\text{Reset}}$ is LOW, $\overline{\text{Blanking}}$ is LOW.

During normal game operation, PA2 outputs a steady PDC signal with a period of about .8 msec. This signal' is buffered by IC7 and AC coupled to the blanking circuit via C32. Positive transitions cause a +9V pulse to appear at Q5's base. This does not affect the circuit, Negative transitions cause a +1 volt pulse on Q5's base and the trigger input. The trigger input now resets the internal flip-flop, turning OFF the Q and discharge outputs HIGH and OFF, respectively. Q5 is turned ON and discharges C31 to about 1.6 volts After the pulse, Q5 is OFF but R22 can only recharge C31 to about 2.6 volts before the next negative transition occurs.

The two diagnostic switches in the front door connect to the CPU board through connector 1J4. In the old board, the IRQ line strobed the front door switches. The switch returns were inverted by NAND gates at IC24. In the new boards, the switches are connected to ground and NOR gates at IC5 act as input buffers. In both cases, the MPU is not interrupted. Instead, the CA1 and CB1 inputs are used as input latches. The MPU reads the internal registers of PIA I to see if any switch data is clocked in to the PIA from the front door diagnostic switches.

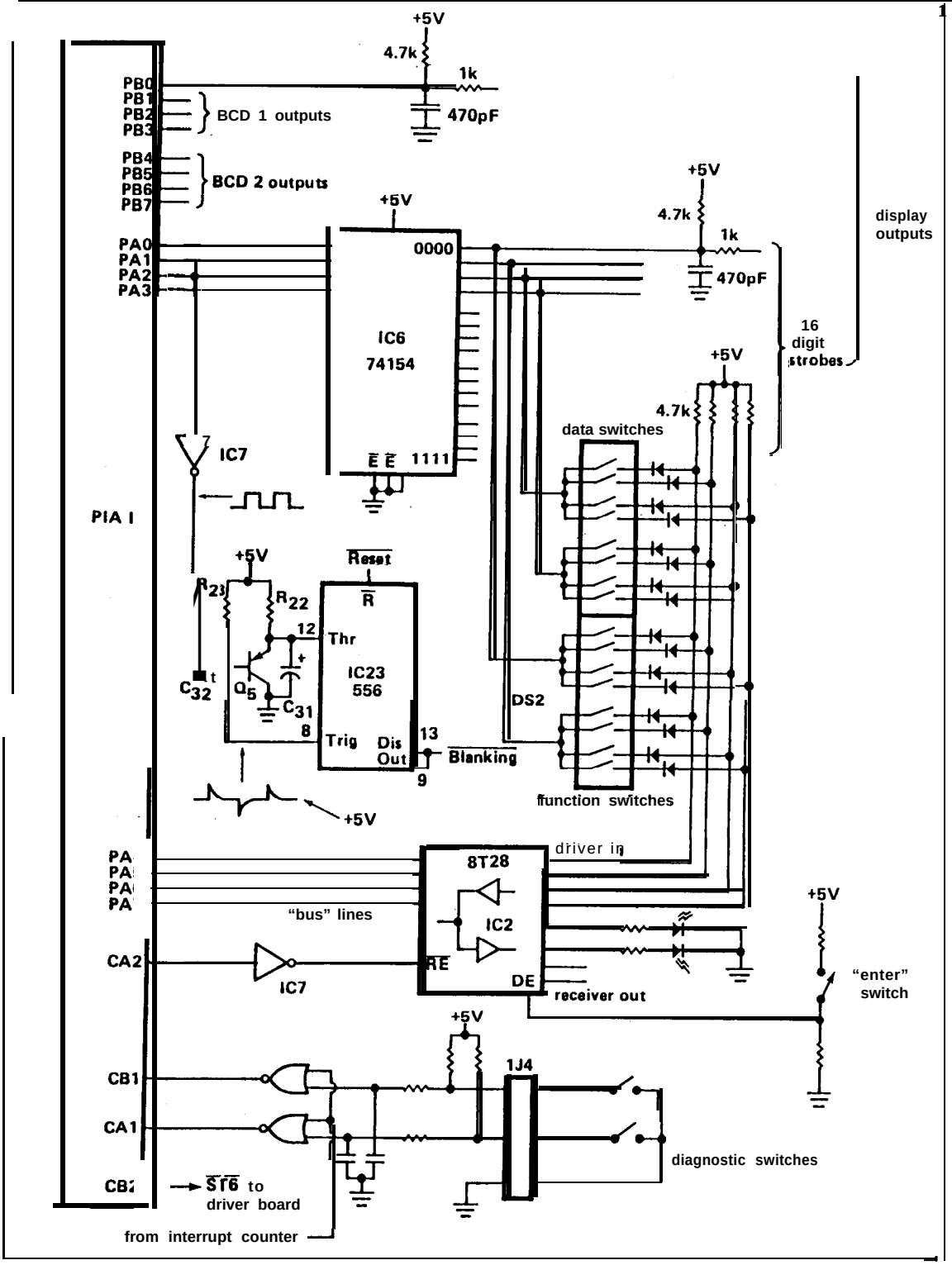
The CB2 output is the ST6 signal which is used by the solenoid driver circuits.



4. THE DRIVER BOARD

PIA II Ports — The Switch Matrix

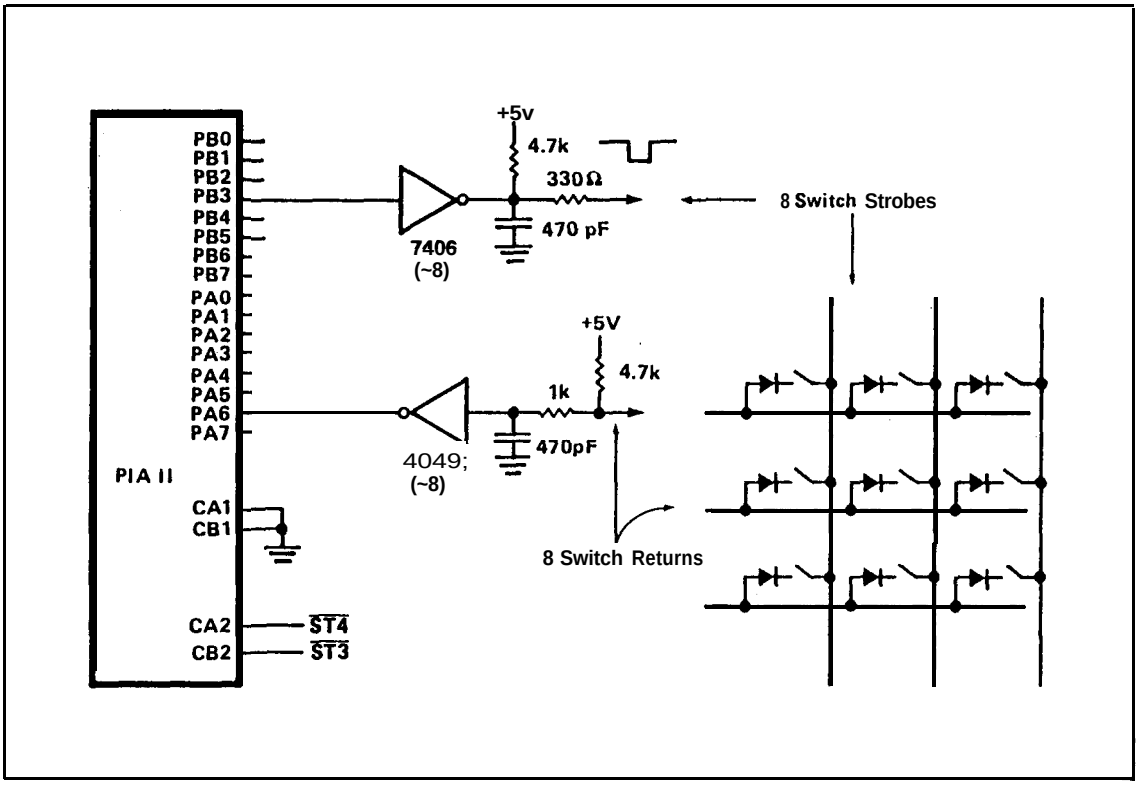
PIA II, at IC11 of the driver board, controls the 64 position playfield and cabinet switch matrix. Williams call their switch strobe lines "drive lines" or "switch columns". The returns are "inputs" or "rows".


+5V
4.7k
1k
470pF
PB0
PB1
PB2
PB3
BCD 1 outputs
PB4
PB5
PB6
PB7
BCD 2 outputs
PA0
PA1
PA2
PA3
0000
IC6
74154
1111
display
outputs
16
digit
strobes
data switches
IC7
PIA I
Reset
R23
R22
12
Thr
IC23
556
C32
Q5
C31
8
Trig
Dis
Out
13
9
Blanking
DS2
function switches
driver in
8T28
IC2
"bus" lines
CA2
RE
DE
receiver out
"enter"
switch
CB1
CA1
1J4
diagnostic switches
CB2
ST6 to
driver board
from interrupt counter

Column 1 of the switch matrix strobes the front door and cabinet switches. Columns 2 through 8 are available for use on the playfield. The eight row returns are used in parallel in both the cabinet and playfield and the two sets are tied together physically at 2J3 on the upper right hand side of the driver board. Connector 2J2 above it carries the output strobes.

The switch matrix uses LOW strobing controlled by the PB ports of PIA II. 7406 open collector, high voltage output inverters are used to drive the strobe lines.

The switch returns, or rows, are inverted with CMOS 4049B inverters. The use of CMOS returns provides a higher input LOW threshold voltage than if TTL inputs were used. Thus, the 0.6V drop of the switch diode plus the 0.4V drop of the 7406 output transistor is 1.OV, which is well below the 1.5V CMOS LOW threshold. The outputs of the CMOS inverter are read by the PA ports of PIA I I.



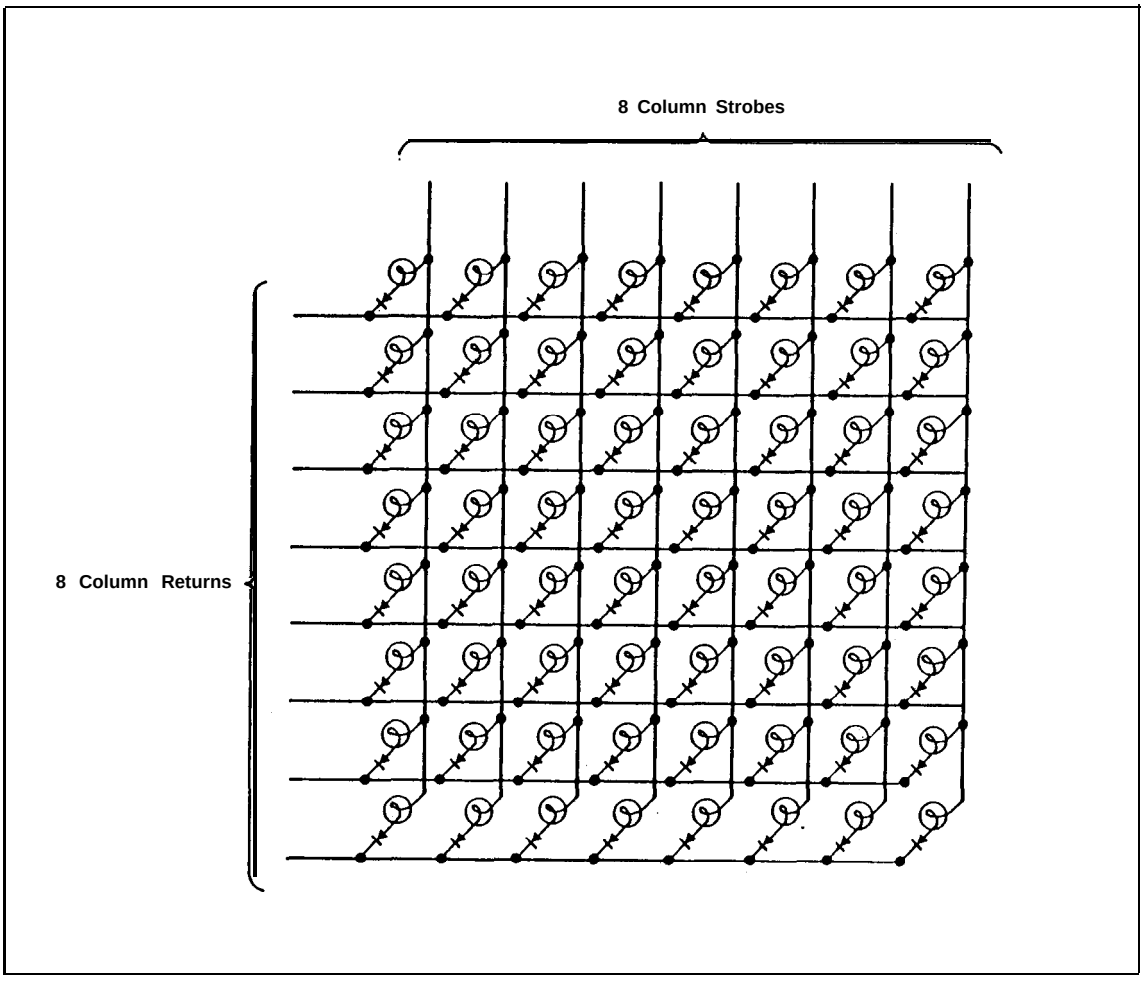
Both the strobe and return lines use 470pF capacitors, 4.7k pull-up resistors and 1 k series resistors. These deglitch the lines, provide static protection and provide momentary protection to both the strobes and returns in the event of accidental shorts on the playfield to lamps or solenoids.

Note also that return continuity can be checked with a voltmeter and should measure at 5 volts with open switches.

The CB2 and CA2 outputs control the ST3 and ST4 signals which are used. by the solenoid driver circuits. CA1 and CBl are not used.

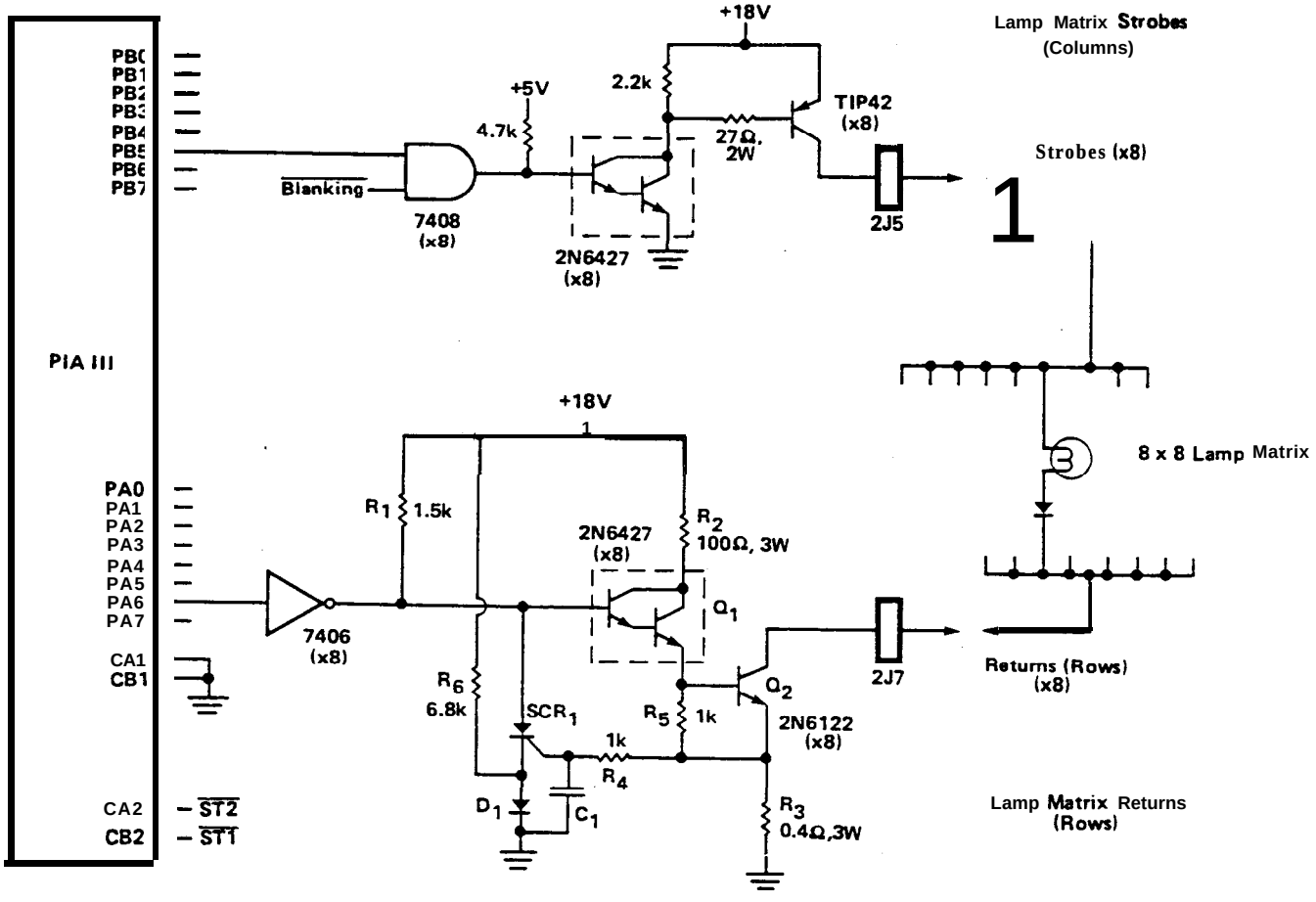
A III Ports – The Lamp Matrix

The Williams lamp drivers are a matrixed system with eight strobe or column lines and eight return or row lines providing control over a maximum of 64 positions in the switched lamp matrix. Each matrix position is capable of driving 3 individual lamps, but a maximum of 10 lamps can be wired to any column, and 10 lamps wired to any row. Columns 1 through 6 and two positions of column 7 are available for playfield lamps. The other 14 matrix positions are reserved for use behind the backglass.



In operation, one strobe line is raised HIGH at a time and the eight different return lines may or may not be pulled LOW, turning ON individual lamps. Note that up to eight positions at a time are powered by the strobe line but only one position is controlled by each return line at a time. The voltages chosen for the system pulse about 11 watts of power to each lamp but for only 12½% (1/8th) of the time. On an average basis, this works out to about 1.4 watts per bulb, about 0.2 watts less than the rating for No. 44 bulbs. A diode is wired in series with each lamp position to prevent current from backing its way through the matrix.

Connector 2J5 on the bottom of the driver board connects the ten yellow strobe


PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PIA III
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CA1
CB1
CA2
CB2
ST2
ST1
Blanking
7408
(x8)
+5V
4.7k
+18V
2.2k
27Ω, 2W
TIP42
(x8)
2N6427
(x8)
2J5
Lamp Matrix Strobes
(Columns)
Strobes (x8)
1
8 x 8 Lamp Matrix
+18V
1
R1 1.5k
7406
(x8)
2N6427
(x8)
R2
100Ω, 3W
Q1
2J7
Returns (Rows)
(x8)
R6
6.8k
SCR1
1k
R4
R5 1k
Q2
2N6122
(x8)
D1
C1
R3
0.4Ω,3W
Lamp Matrix Returns
(Rows)

(column) lines to the playfield and insert board. Connector 2J7 connects the sixteen red 'urn (row) wires to the driver board.

The PB lines of PIA III, at IClO, control the eight identical column drivers. When LOW, the PB lines turn the strobe lines OFF. The Blanking signal from the CPU board is ANDed by a 7408 AND gate with each PB output. When Blanking is LOW, all the lamps are OFF. The output of each AND gate controls a 2N6427 medium current NPN Darlington transistor. A 4.7k pull-up resistor provides the base current for the Darlington.

When the Darlington is ON, it provides base current via a 27Ω, 2 watt resistor to the type TIP42 PNP high current driver transistor which turns fully ON, raising the strobe line to within 0.4V of the +18V lamp supply. When the PB output goes LOW, the output of the AND gate'is LOW, the Darlington is OFF, and the 2.2k resistor helps keep the driver turned fully OFF.

Also illustrated is one of the eight identical return or row drivers. The component numbers are different in the actual game. The row driver features a short circuit protection built around an SCR.

The PA ports of PIA III control eight 7406 high voltage, open collector inverters. R1 is a pull-up resistor tied to the +18V supply and provides the base current for QI, a 2N6427 type Darlington when the output transistor of the inverter is OFF. When QI is turned ON, it provides base current for Q2, the high current NPN row driver transistor, pulling the return line LOW, illuminating a lamp. R2 provides collector current for QI.

The emitter voltage of Q2 is defined by Ohm's Law and the current flowing through R3. The driver only turns ON one lamp matrix position at a time and the current flow, assuming No.44 lamps, will be about 0.6A per lamp during each pulse. The voltage on R3 will therefore be 0.4 x 0.6V = 0.24 volts/lamp. There is a 0.6 volt drop across each of the three base-emitter junctions in this circuit, so the voltage at the base of QI will therefore 0.24V + 2.4V = 2.64V. The voltage on the gate of SCR1 will be 0.24V by virtue of its connection to R3 via R4. D1 and R6 keep the cathode of SCR1 at 0.6V, meaning that the SCR will be in the OFF state during these conditions.

If a short in the matrix occurs, a large current will flow through R3, creating a larger than normal voltage drop across it. If R3's voltage reaches around 1.3V (over 3A), R4 can supply enough gate current to SCR1 to switch it into its ON state. Cl deglitches the gate of SCR1. With the SCR ON, the base of QI is clamped down to about 1.4 volts. R5 helps pull the emitter voltage of QI down to about 0.5 volts and turns Q2 fully OFF.

At the end of the ON pulse from the PA ports, the output transistor of the inverter pulls the anode of SCR1 down to 0.4V, which causes the SCR to switch immediately into its OFF state. The next lamp column is then strobed and the row driver may or may not be switched ON by the MPU.

If a short in a lamp, a socket, or the wiring does occur, only the lamp position with the problem will be detected by the driving circuits; none of the other lamps in the matrix would be affected. Only a short duration (0.14μsec) pulse will occur through the short. No other circuit component would be affected.

PIA IV Ports – Solenoid Control

PIA IV is used to control 22 different solenoid driver transistors and a flipper relay. There are basically three circuit configurations. The first is the processor only controlled

drivers of which there are sixteen. The second is the flipper circuit and the third is the special solenoid drivers of which there are six.

The sixteen PA and PB ports of PIA IV are used as outputs to control the sixteen processor only controlled drivers. Each port output is first ANDed with the Blanking signal with 7408 AND gates (IC1, IC2, IC3 and IC4). The port output must be HIGH to turn ON a coil. If the Blanking signal is pulled LOW, the solenoids are all OFF.

The outputs of the AND gates control a 2N4401 NPN buffer transistor. A 560 Ω resistor provides base current for this transistor. Collector current for it is supplied by a 68 Ω resistor. When ON, the transistor provides the base current for a type TIP120 NPN Darlington driver transistor, turning it ON. The TIP120s provide the ground returns for the 'sixteen processor only controlled solenoids. Note that the driver ground is the same as the logic ground. The 2.7k resistor helps keep the TIP120 turned fully OFF when it is supposed to be. Connectors 2J9 and 2J11 provide the connections to the coil return wires.

The C82 output of.PIA IV is the Game On output signal to the rest of the drivers. When this line is HIGH, a game is in play. The Game On signal is ANDed with the Blanking signal with an AND gate of IC7. A 7402 NOR gate, IC9C, is wired as an inverter and connects to the output of this AND gate. Now, if either Game On or Blanking goes LOW, the output of this NOR gate will 'go HIGH, signalling the other seven drivers to go OFF.

Another 7402 NOR gate, IC8A, inverts this signal again. When both Game On and Blanking are HIGH, the output turns Q13 ON which energizes flipper relay Z1. R25 provides base current to Q13. R26 and R27 provide additional despiking control on the relay coil. In the event of failure of D1, the additional loading helps prevent voltage spikes from the coil from entering the +5 volt supply.

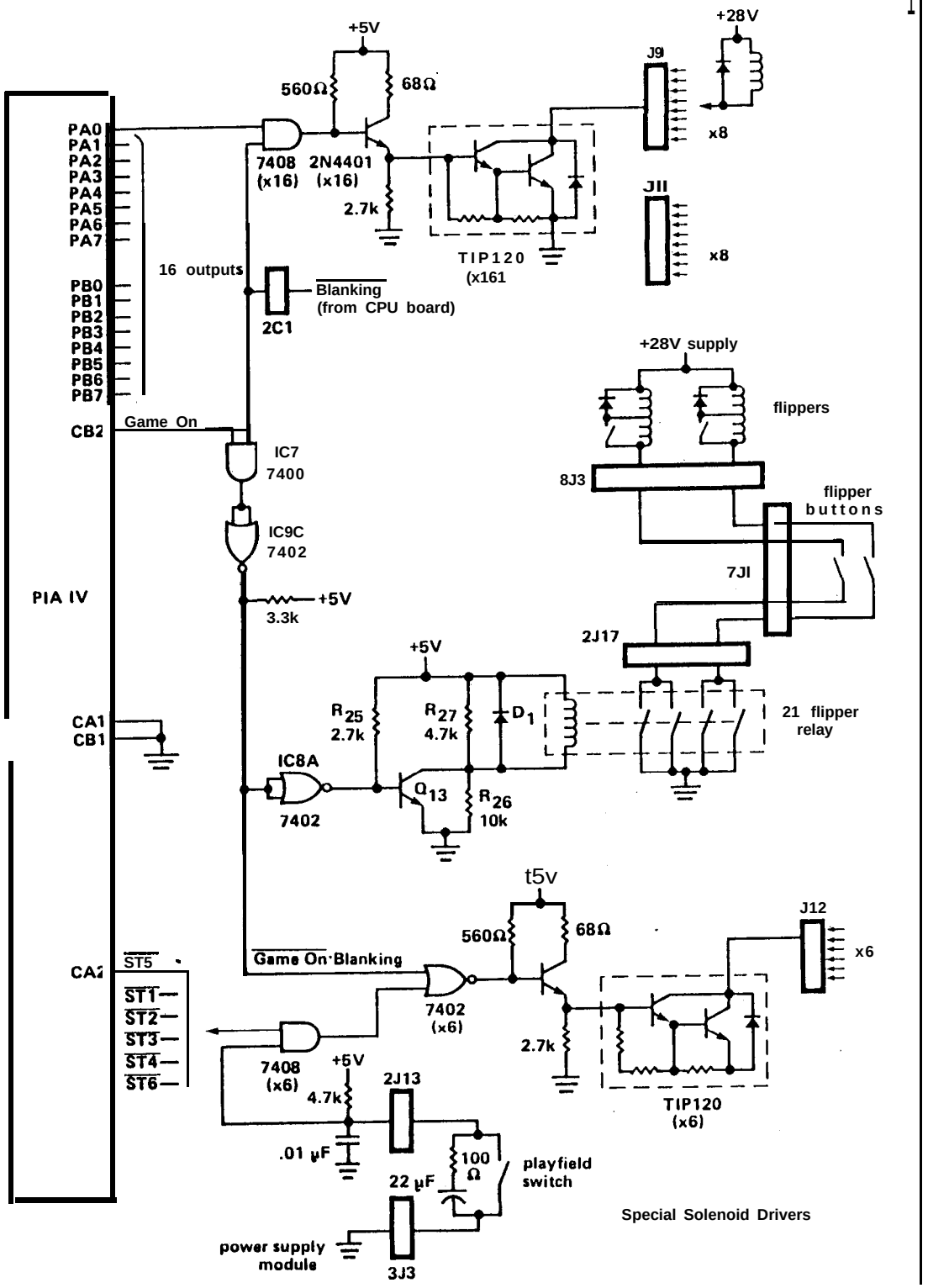
When the relay is ON, the ground return circuits are completed to the flipper buttons in the cabinet. If they are pressed, the flipper coils will energize.

The third set of solenoid drivers are the special solenoid drivers: The actual buffer and driver transistors and associated resistors are identical to the sixteen processor only controlled drivers. The differences lie in the buffer circuits. The special solenoid drivers can be controlled by either the PIA ports or by playfield switches.

Six of the eight CA2 and CB2 ports of PIAs I through IV are used as special solenoid strobe outputs and are called $\overline{ST1}$ through $\overline{ST6}$. These are normally HIGH but go LOW to turn ON one of these solenoids.

There are also six special switch inputs which have pull-up resistors on the driver board but can be pulled LOW on the playfield by playfield switches and this also turns ON a coil. The 100Ω resistor and 22μF, 15V capacitor are used to extend the length of time that a coil is energized.

Both the $\overline{STx}$ lines and switch inputs are ANDed by a 7408 AND gate (IC6 and IC7). If either of the two input lines go LOW, the output will go LOW. The output is NORed with the Game On-Blanking output of IC9C by a 7402 NOR gate (IC8 and IC9). Both inputs must be LOW in order for there to be a H IGH output which turns ON a driver transistor in the same manner as the processor only controlled solenoid drivers.


+5V
560Ω
68Ω
+28V
J9
x8
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
7408 (x16)
2N4401 (x16)
2.7k
TIP120 (x161
J11
x8
16 outputs
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
Blanking (from CPU board)
2C1
+28V supply
flippers
8J3
flipper buttons
7J1
CB2
Game On
IC7
7400
IC9C
7402
PIA IV
+5V
3.3k
2J17
+5V
R25 2.7k
R27 4.7k
D1
21 flipper relay
CA1
CB1
IC8A
7402
Q13
R26 10k
t5v
560Ω
68Ω
J12
x6
CA2
ST5
Game On·Blanking
ST1
ST2
ST3
ST4
ST6
7402 (x6)
2.7k
7408 (x6)
+5V
4.7k
2J13
TIP120 (x6)
.01 µF
100 Ω
playfield switch
22 µF
power supply module
3J3
Special Solenoid Drivers