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CAT BOX / Z8002 INTERFACE

USERS GUIDE

A Warner Communications Company

Z8002 Interface Users Guide

Introduction

The Z8002 Interface is designed to adapt the ATARI CAT Box for troubleshooting the Z8002 16-bit microprocessor and associated circuitry. This Users Guide contains: (1) troubleshooting procedures, (2) illustrated parts lists, and (3) a schematic diagram. The preliminary procedure for setting up the Z8002 for testing a game PCB is included in this manual and on the cover of the Z8002 Interface.

The Z8002 microprocessor and its associated circuitry is tested similarly to other microprocessors. The Z8002 Interface allows the testing of 16 data lines. The following tests are recommended, in the order of importance, for locating a faulty microprocessor or associated circuitry:

- **RAM Test.** The RAM test is the most powerful test that can be performed with the ATARI CAT Box. A positive RAM test indicates that the data lines, data buffers, address lines, address buffers, RAM, RAM enables, and any interface components (e.g., custom integrated circuits) between the microprocessor and the RAM are operating properly.
- **ROM Test.** The ROM test determines the condition of the ROM, ROM enables, and address lines.

Preliminary Procedure

1. Turn off the electrical power to the game.
2. Connect the CAT Box 50-pin flat cable and the Z8002 Interface 40-pin flat cable as shown on the label attached to the Interface cover.
3. Remove the printed-circuit board (PCB) under test from the game.
4. Remove the Z8002 microprocessor from its socket.
5. Insert the Z8002 Interface 40-pin IC socket connector into the empty Z8002 socket. Make sure the Z8002 Interface 40-pin IC-socket connector pins mate with the corresponding contacts on the empty Z8002 socket.
6. Connect the game harness(es) to the PCB under test.
7. Apply power to the game and the CAT Box.

RAM Test

1. Set the Z8002 Interface RAM/ROM switch to RAM (the L BYTE/H BYTE switch is not used for this test).
2. Set the CAT Box switches as follows:

R/$\overline{W}$ MODE	(OFF)
R/$\overline{W}$	WRITE
ERROR DATA DISPLAY	GAME
BYTES	1024 (for 10 address lines) 256 (for 8 address lines)
TESTER MODE	R/$\overline{W}$
CHECKSUM	OFF

3. Determine the starting RAM address from the Memory Map provided in the Schematic Package Supplement for the PCB under test.
4. Ground the $\overline{RESET}$ test point on the PCB under test.
5. Press the TESTER RESET pushbutton.
6. Type in the starting address on the CAT Box keyboard.
7. Set the R/$\overline{W}$ MODE switch to PULSE and then back to (OFF).
8. Set the R/$\overline{W}$ switch to READ.
9. Set the R/$\overline{W}$ MODE switch to PULSE and then back to (OFF).
10. Check that the COMPARE ERROR LED indicator *is not* lit and that the ADDRESS/SIGNATURE readout indicates an address increment of 400 (for 1024 bytes) or 100 (for 256 bytes). For example, a starting address of 4000 will increment to 4400 for 1024 bytes or 4100 for 256 bytes. If this test is positive, proceed to step 11. If the COMPARE ERROR LED *is* lit, proceed to the RAM Failure procedure.
11. Set the R/$\overline{W}$ switch to WRITE and repeat steps 7 through 10 until the ADDRESS/SIGNATURE readout indicates the highest RAM address listed in the Memory Map.
12. Switch DBUS SOURCE to $\overline{ADDR}$ and repeat steps 3 through 11.

RAM Failure

1. Note the ADDRESS/SIGNATURE and DATA readouts when the COMPARE ERROR LED comes on to indicate a failure.
2. Set the ERROR DATA DISPLAY switch to TESTER and note the DATA readout.
3. Press the TESTER RESET pushbutton.
4. Set the CAT Box switches as follows:

R/$\overline{W}$ MODE	(OFF)
R/$\overline{W}$	WRITE
ERROR DATA DISPLAY	GAME
BYTES	1
DBUS SOURCE	DATA

5. Type in the address on the CAT Box keyboard noted in step 1.
6. Set the R/$\overline{W}$ MODE switch to STATIC and then back to (OFF).

7. Use an oscilloscope or logic probe and check for the following RAM enables:
   a. If no RAM is enabled, check the enable decoder.
   b. If two RAMs are enabled, note the last digit of the ADDRESS/SIGNATURE readout. An even digit (as in 46A4) indicates that the failed RAM involves the lower data lines (D0–D7), an odd digit (as in 46A5) indicates that the failed RAM involves the higher data lines (D8–D15).
   c. If four RAMs are enabled, determine which pair of RAMs is involved as described in part b. Then, determine which data line is incorrect from the data noted in steps 1 and 2. The suspect RAM is the one connected to the incorrect data line.
8. Replace the suspected RAM and perform the RAM Test procedure again. If the same address or data lines are incorrect, a problem exists in the address or data lines. Check the buffers between the CAT Box and the previously replaced RAM.

ROM Test

1. Perform the Preliminary Procedure.
2. Set the Z8002 Interface switches as follows:

RAM/ROM	ROM
H BYTE/L BYTE	H BYTE

3. Set the CAT Box switches as follows:

DBUS SOURCE	DATA
BYTES	1 (for 11 address lines) 256 (for 12 address lines) 1024 (for 13 address lines)
ERROR DATA DISPLAY	GAME
R/$\overline{W}$	READ
R/$\overline{W}$ MODE	(OFF)
CHECKSUM	ON

4. Determine the starting ROM address from the Memory Map provided in the Schematic Package Supplement for the game under test.
5. Ground the $\overline{RESET}$ test point on the PCB under test.
6. Press the TESTER RESET pushbutton.
7. Type in the starting address on the CAT Box keyboard.
8. Switch R/$\overline{W}$ MODE to PULSE and then back to (OFF).
9. Verify that the checksum which appears on the ADDRESS/SIGNATURE readout is correct as compared to a known good PCB, or as listed in the Troubleshooting Guide for the game under test.
10. Repeat steps 5 through 9 for each ROM address listed in the Memory Map.
11. Switch the H BYTE/L BYTE switch on the Z8002 Interface to L BYTE, and repeat steps 4 through 9 for each ROM address listed in the Memory Map.

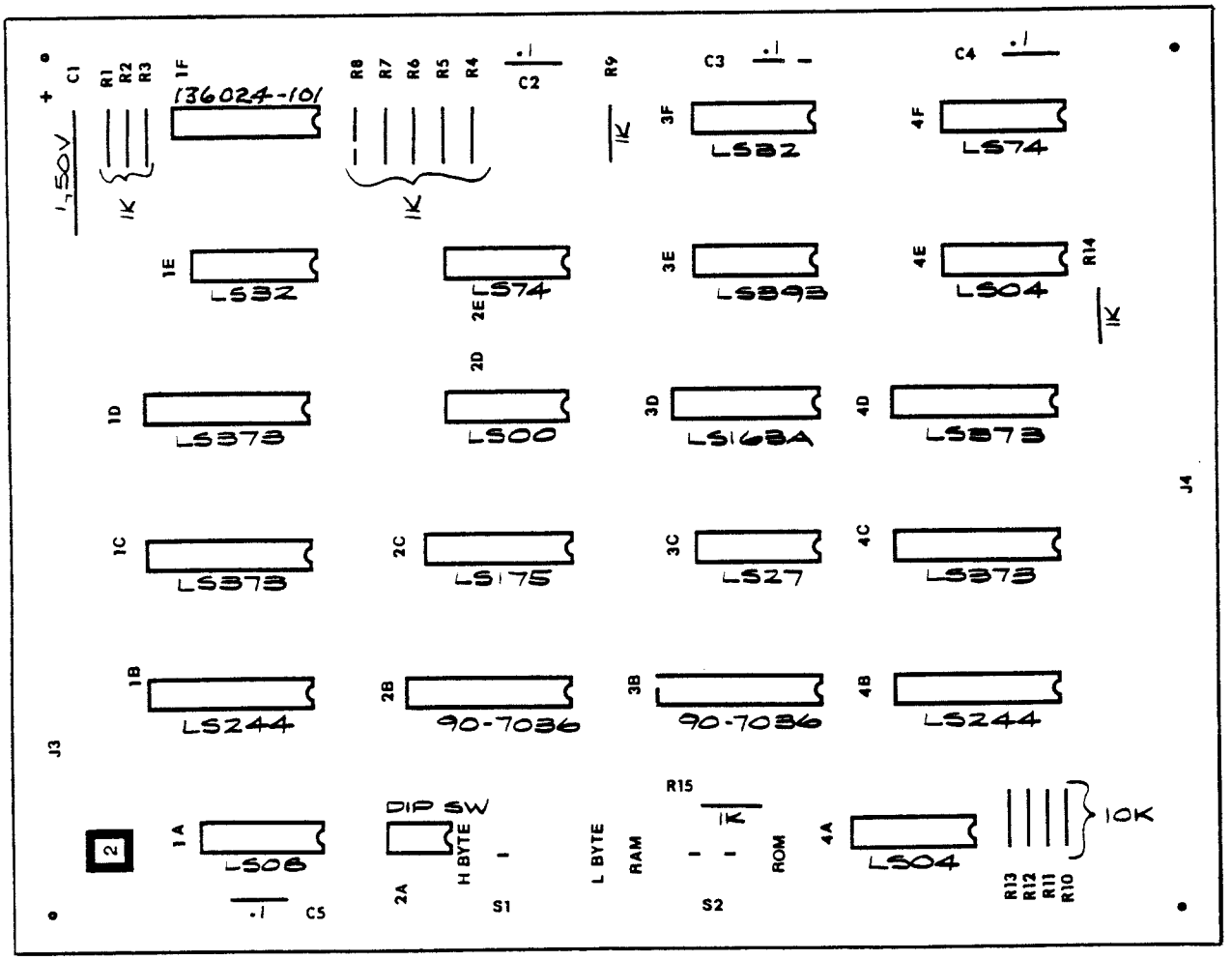

Figure 1 Z8002 Interface Assembly

CAT Box Interface Assembly Z8002 Parts List
A040576-01 2

Designator		Description	Part No.
		Capacitors	
C1		0.1 μF, 50 V, Aluminum Electrolytic, Axial-Lead Ceramic Capacitor	24-500105
C2–C5		0.1 μF, +80%, -20%, 50 V Ceramic Capacitor	122002-104
		Integrated Circuits	
1A		Type-74LS08 Integrated Circuit AND Gate, Quad 2-Input	37-74LS08
1B		Type-74LS244 Integrated Circuit Line Driver/Receiver	37-74LS244
1C		Type-74LS373 Integrated Circuit Octal, D-Type	37-74LS373
1D		Type-74LS373 Integrated Circuit Octal, D-Type	37-74LS373
1F		Type-82S123 PROM Integrated Circuit	136024-101
1E		Type-74LS32 Integrated Circuit OR Gate, Quad 2-Input	37-74LS32
2B, 3B	⚠	Type-2114-2 RAM Integrated Circuit	90-7036
2C		Type-74LS175 Integrated Circuit Flip-Flop, Quad D-Type	37-74LS175
2D		Type-74LS00 Integrated Circuit NAND Gate, Quad 2-Input	37-74LS00
2E		Type-74LS74 Integrated Circuit Flip-Flop, Dual D-Type	37-74LS74
3C		Type-74LS27 Integrated Circuit NOR Gate, 3-Input	37-74LS27
3D		Type-74LS163A Integrated Circuit Counter, Sync 4-Bit	37-74LS163A
3E		Type-74LS393 Integrated Circuit Counter, Dual 4-Bit	37-74LS393
3F		Type-74LS32 Integrated Circuit OR Gate, Quad 2-Input	37-74LS32
4A		Type-74LS04 Integrated Circuit Hex Inverter	37-74LS04
4B		Type-74LS244 Integrated Circuit Line Driver/Receiver	37-74LS244
4C, 4D		Type-74LS373 Integrated Circuit Octal, D-Type	37-74LS373
4E		Type-74-LS04 Integrated Circuit Hex Inverter	37-74LS04
4F		Type-74LS74 Integrated Circuit Flip-Flop, Dual D-Type	37-74LS74
		Resistors	
R1–R9		1.0 kΩ, ±5%, ¼ W Resistor	110000-102
R10–R13		10 kΩ, ±5%, ¼ W Resistor	110000-103
R14, R15		1.0 kΩ, ±5%, ¼ W Resistor	110000-102
		Miscellaneous	
1F		16-Pin Medium-Insertion Force IC Socket	79-42C16
2A		4-Toggle DIP Switch	66-114PIT
2B, 3B		18-Pin Medium-Insertion Force IC Socket	79-42C18
S1, S2		SPDT Rocker Switch	160030-103

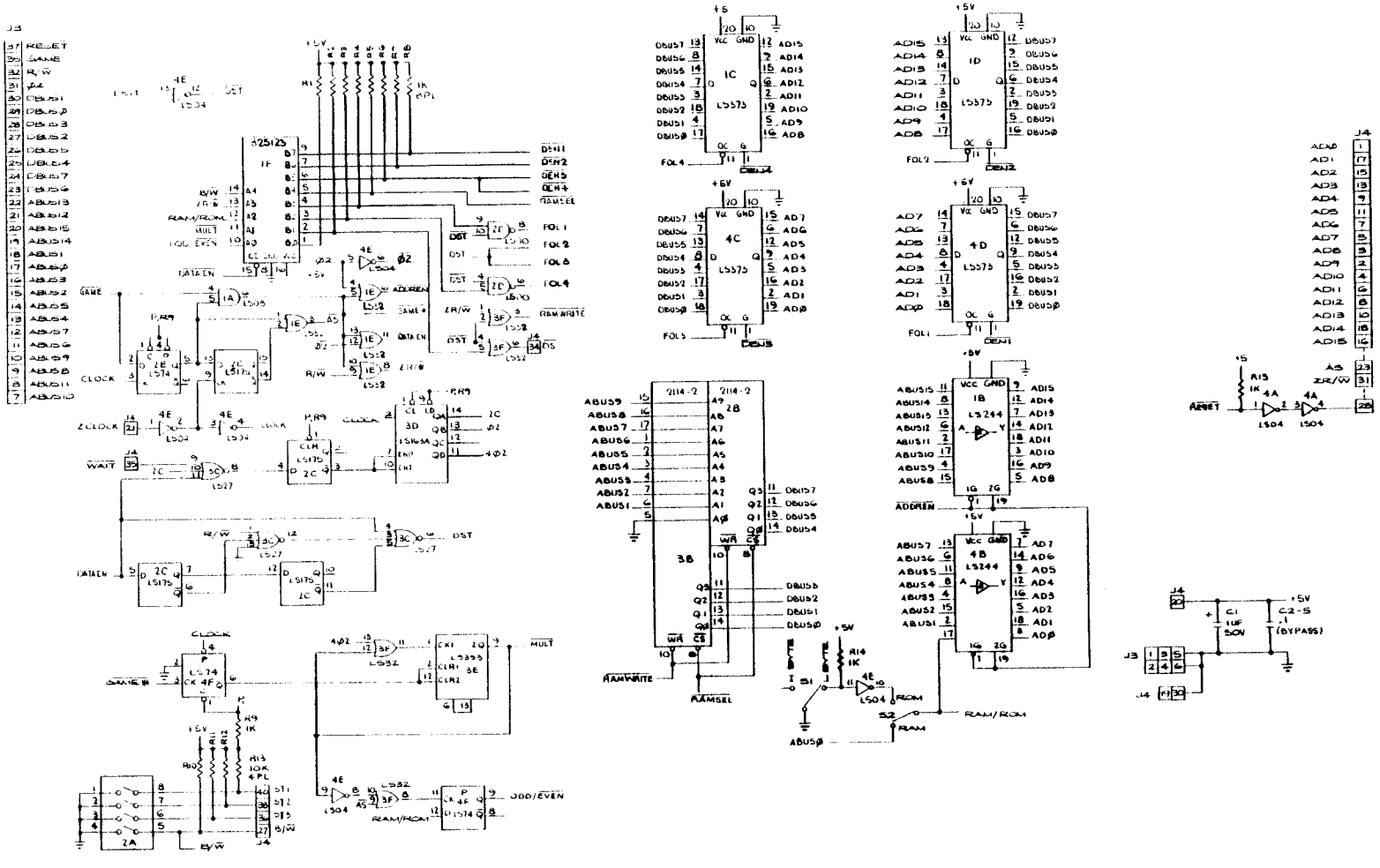

Figure 2 Z8002 Schematic Diagram

A Warner Communications Company

ATARI, INC.
790 Sycamore Drive
P.O. Box 906
Milpitas, California 95035
408/942-3100 • TELEX 35-7488