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9100 Series

Service Manual

P/N 809210
May, 1988

FLUKE®

LIMITED WARRANTY

John Fluke Mfg. Co., Inc. (Fluke) warrants your 9100/9105A to be free from defects in material and workmanship under normal use and service for 90 days from the date of shipment. Software and firmware products are provided "AS IS." We do not warrant that software or firmware products will be error free, operated without interruption or that all errors will be corrected. This warranty extends to you if you are the original purchaser and does not apply to fuses, batteries or any product which, in our sole opinion, has been subject to misuse, alteration or abnormal conditions of operation or handling.

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Fluke will, at our option, repair or replace the defective product free of charge. However, if we determine that the failure was caused by misuse, alteration, or abnormal condition of operation or handling, you will be billed for the repair. The repaired product will be returned to you, transportation prepaid.

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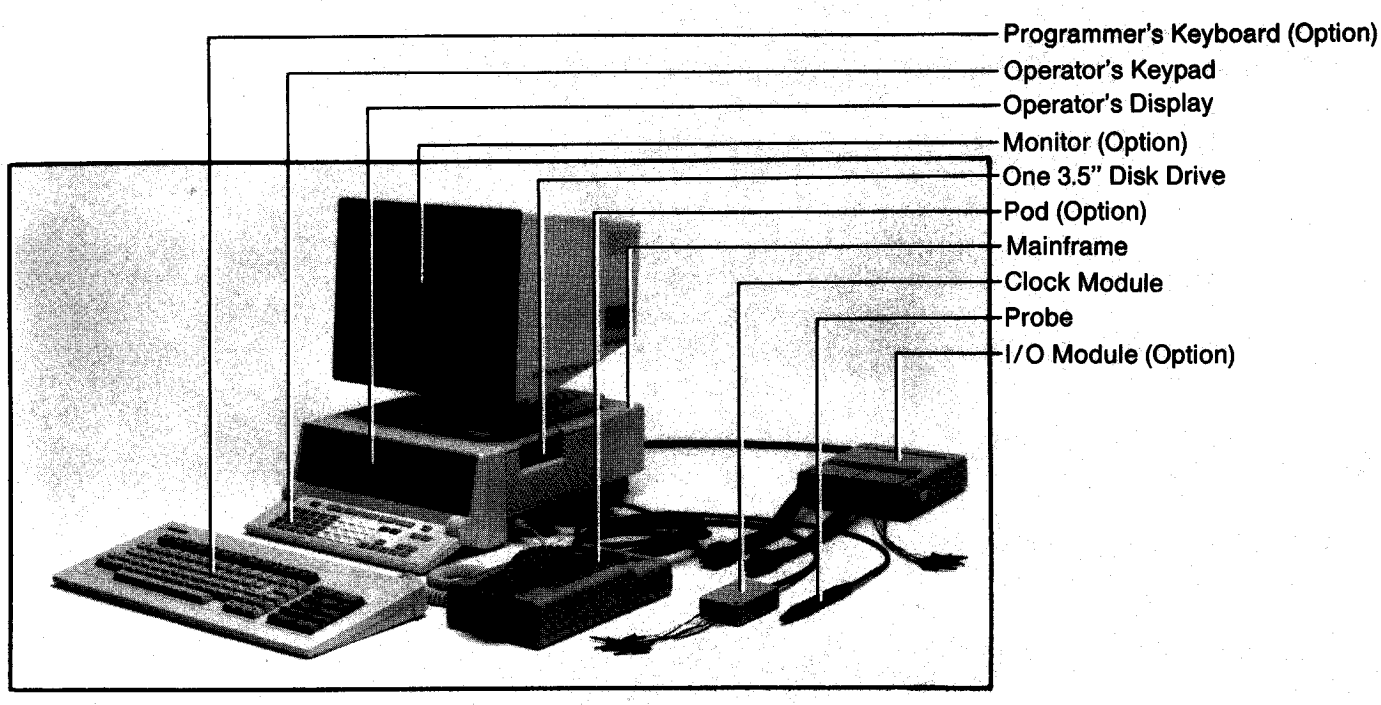
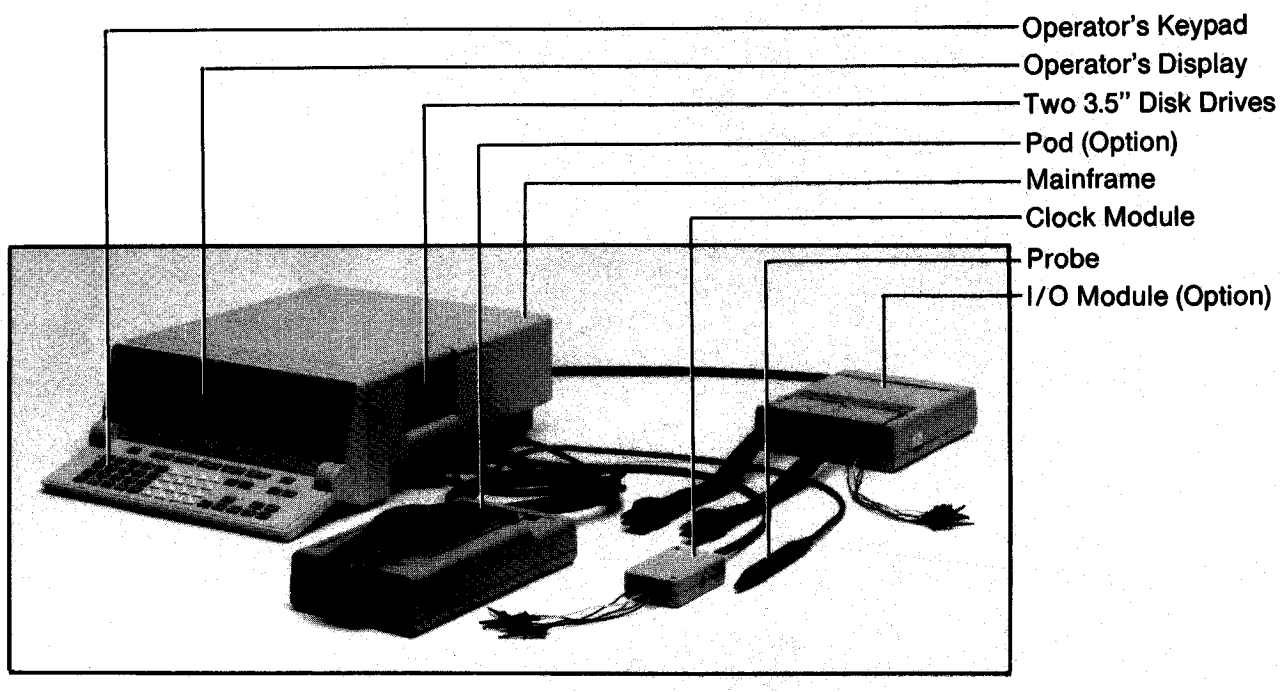


9100A System



9105A System

Section 1
How to Use This Manual

CONTENTS

INTRODUCTION

The 9100A/9105A Service Manual provides overall service and maintenance information. It includes a comprehensive operational theory discussion, along with replacement parts lists and schematic diagrams. The Service Manual offers a detailed and technical description of the 9100A and 9105A and, when used with the 9100A/9105A Service Kit, can be used during troubleshooting procedures. This manual covers both standard mainframes and optional assemblies.

This Manual

This manual documents issues encountered when servicing and repairing the 9100A/9105A. Other volumes of the 9100A/9105A manual set cover operating and programming the 9100A and using the 9105A. The 9100A/9105A Service Manual consists of the following sections:

Section 1: How to Use This Manual

This section introduces the Service Manual. It also defines some conventions used throughout the manual set.

Section 2: General Information

This section contains various types of often-used information. For quick reference, general descriptions of the instrument, its features, and its power requirements are given. Differences between the 9100A and the 9105A are mentioned. Test equipment called for in the rest of this manual is specified. Shipping and service procedures and addresses are also provided in this section.

Section 3: Theory of Operation

This section describes the 9100A/9105A in terms of major functional areas (termed blocks). Often, an individual functional block is further examined in terms of its own functional blocks. Where necessary, individual components are mentioned in describing the operation of a block and its relationship to other blocks. This information can be used with the schematic diagrams (found later in this manual) during troubleshooting.

Section 4: Maintenance

In addition to describing operator maintenance and adjustments, this section documents procedures required when disassembling, adjusting, or testing the 9100A/9105A. Section 4 also describes reassembly and interconnection of system units.

Section 5: List of Replaceable Parts

This section presents complete ordering information for any part that can be ordered separately.

Section 6: Appendices

This section lists reference information not found elsewhere in the manual. Federal Supply Codes and Manual Status Information are included here.

Section 7: Schematic Diagrams

This section contains schematic diagrams and reference designator drawings for each assembly (standard and optional) used in the 9100A/9105A.

The Manual Set

Other manuals in the 9100A/9105A manual set are:

- Getting Started

  Describes functions and interconnections of the elements of a 9100A or 9105A system.

- Automated Operations Manual

  Describes the use of pre-programmed test or troubleshooting procedures.

- Technical User's Manual

  Describes the use of the 9100A/9105A keypad to test and troubleshoot a Unit Under Test (UUT).

- Applications Manual

  Describes how to design test and troubleshooting procedures for a Unit Under Test (UUT).

- Programmer's Manual

  Describes how to use a 9100A programming station to create automated test and troubleshooting procedures.

- TL/1 Reference Manual

  A complete, alphabetical reference of the TL/1 programming language commands.

CONVENTIONS

Throughout the manual set, certain notational conventions are used. A summary of these conventions follows:

- Instrument Reference

  Usually, a description applies to circuits found in both the 9100A and the 9105A. The instrument is then designated "9100A/9105A". If a description applies to one instrument only, either "9100A" or "9105A" is used.

- Printed Circuit Assembly

  The term "pca" is used to represent a printed circuit assembly and its attached parts.

- Signal Logic Polarity

  Signal names followed by a "-" are active (or asserted) low. Signals not so marked are active high.

- Circuit Nodes

  Individual pins or connections on a component are specified with a dash (-) following the component reference designator. For example, pin 19 of U30 would be U30-19.

- Keystroke Notation

  The following conventions are used to identify syntax keystrokes and differentiate them from surrounding text:

  (xxx) When associated with a keyword, a lower-case word in parentheses indicates an input required by the user.

  XXX An uppercase word without parentheses indicates a literal keyword to be entered by the user.

  <XXX> Angle brackets around all upper-case letters means press the <XXX> key.

CONTENTS

DESCRIPTION

Information brought together in this section serves as a one-source reference for servicing the 9100A, 9105A, and related options. The 9100A/9105A instruments are fully described elsewhere in the manual set. Specifically, Getting Started and the Technical User's Manual can be consulted for hardware and capabilities information.

Power Requirements

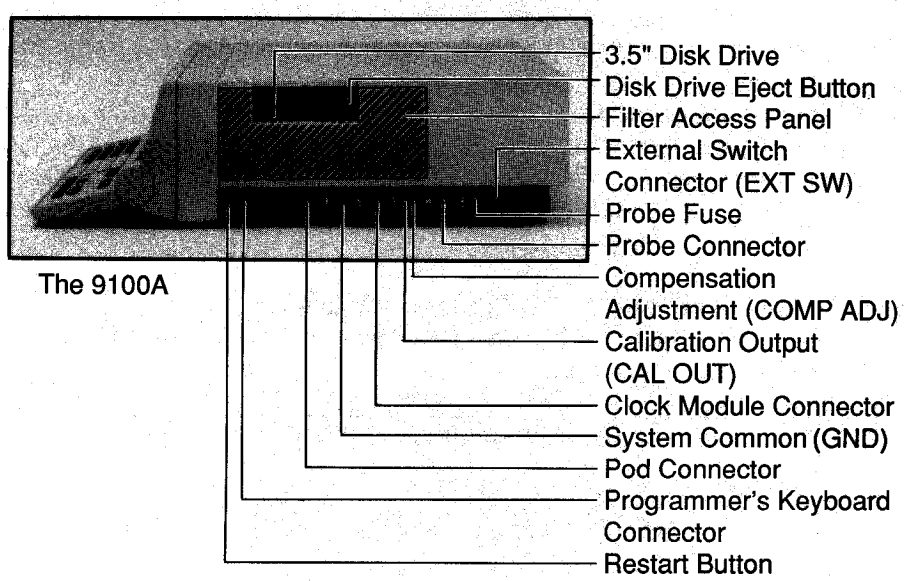
Power requirements for the 9100A/9105A are presented in Table 2-1. The 9100A/9105A mainframe uses a maximum of 150 watts. In addition, the Monitor uses 50 watts maximum.

Table 2-1. Power Requirements

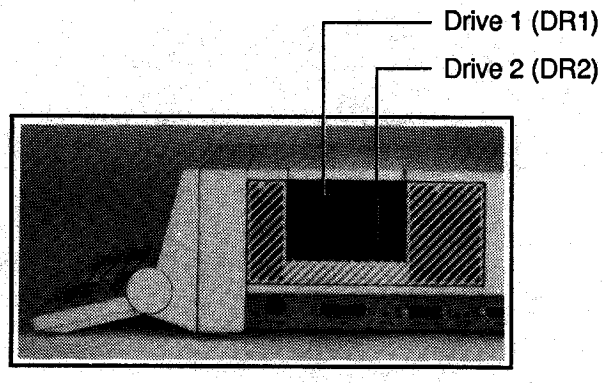
VOLTAGE SWITCH SETTING	LINE VOLTAGE RANGE	FREQUENCY	FUSE
110V	90-130V ac	47 to 440 Hz	2A Slow Blow
220V	180-264V ac	47 to 63 Hz	1A Slow Blow

External Connections

Servicing the 9100A/9105A may require disconnection of system components. For ease of reassembly, full connection information is presented here. Figure 2-1 identifies connections and other features found along the right side of either instrument. Figure 2-2 shows rear panel features.



The 9100A



The 9105A, showing its different disk drive arrangement.

Figure 2-1. Side Features

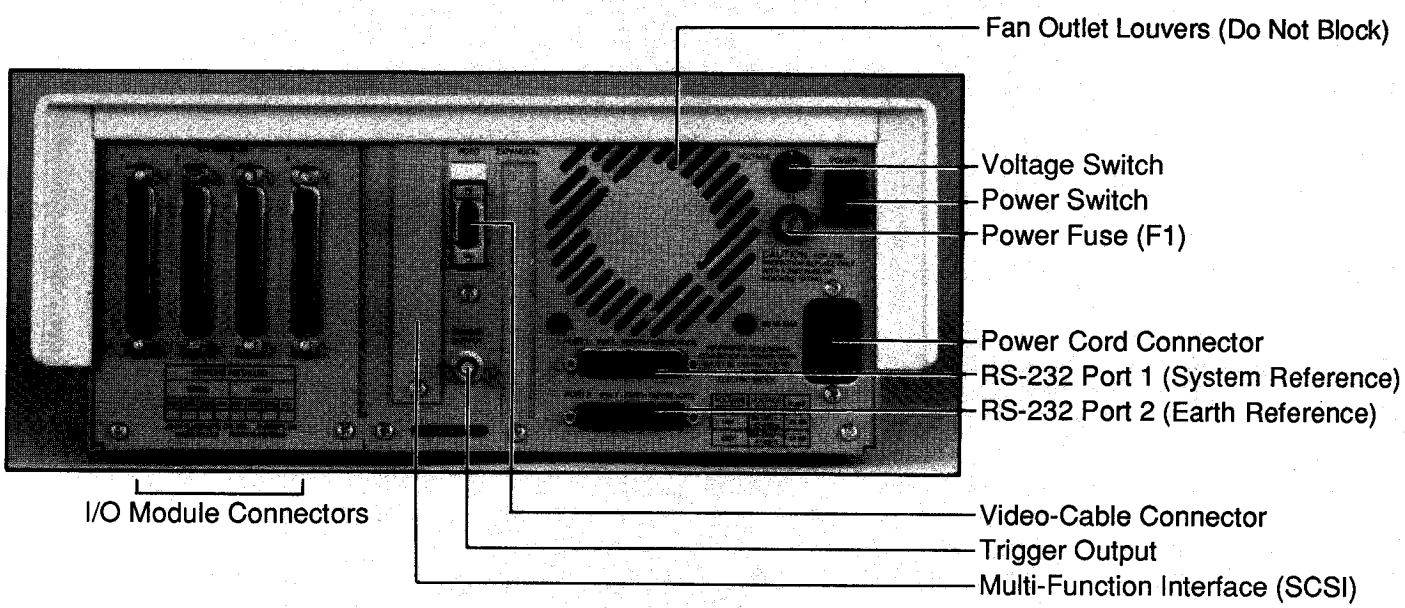


Figure 2-2. Rear Panel Features

SYSTEM COMPONENTS

Theories of operation, maintenance instructions, and schematic diagrams in this manual cover all 9100A/9105A system components. Refer to other manuals in the 9100A/9105A manual set for complete descriptions and usage instructions. The Getting Started manual provides a good overview of system components. These are listed and categorized in the following paragraphs, with references to coverage within this manual.

9100A Systems

The 9100A Digital Test System constitutes the mainframe, probe, and clock module documented in this manual.

The 9100/SYS Digital Test Programming System includes 9100A Test System components, along with the 9100A-003 Parallel I/O Module, the 9100A-004 Programmer's Station, and the Y9100A-DCS DIP Clip Set accessory described in this manual.

9105A System

The 9105A Test Station includes the mainframe, probe, and clock module described in this manual.

Options

The 9100A-004 Programmer's Station applies to the 9100A only. Its monochrome monitor, monochrome video controller, and keyboard are documented in this manual.

The 9100A-005 Programmer's Station is also available for the 9100A only and provides the color video controller and keyboard described in this manual.

Option 9105A-008, Real-Time Clock and Option 9105A-007, 512K Expansion Memory, are available for the 9105A only and are documented in this manual.

Finally, the following options are available for either the 9100A or the 9105A and are separately documented in this manual:

- Parallel I/O Module, Option 9100A-003, includes a Y9100A-20L Flying Lead Module and a Calibration Module.
- Video (Monochrome), Option 9100A-009, includes a Video Controller and a Monochrome Monitor.
- Video Controller (Color), Option 9100A-011.
- Keyboard, Option 9100A-013

Accessories

All hardware accessories for the 9100A/9105A are documented in this manual. These include:

- Half-Width Clip Modules, Accessories Y9100A-14D, -14S, -16D, -16S, -18D, 20D, 20S, -24D, and 24S.
- Full-Width Clip Modules, Accessories Y9100A-28D, -28S, and -40D.
- Y9100A-DCS DIP Clip Set, including Y9100A-14D, -16D, -18D, -20D, -24D, -28D, and -40D.
- Flying Lead Module, Accessory Y9100A-20L

Interface Pods

Interface pods can be used with a wide range of microprocessors. Each pod is documented in its own manual, none of which are included with 9100A/9105A Manual Set. No pod information is provided in this service manual.

REQUIRED TEST EQUIPMENT

Tools and test equipment required in servicing the 9100A or 9105A are listed in Table 2-2.

SHIPPING INFORMATION

When you receive the instrument, inspect the shipping container for any possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If it is necessary to reship the instrument, use the original container. If the original container is not available, a new one can be obtained from the John Fluke Manufacturing Co., Inc. upon request.

SERVICE INFORMATION

The 9100A/9105A is warranted for a period of 90 days upon delivery to the original purchaser. The warranty is located in the front of this manual, following the title page.

Factory calibration and service for each Fluke product is available at various locations worldwide. A complete list of these service centers is given in the appendices of this manual. If requested, an estimate will be provided to the customer before any work is begun on an instrument whose warranty period has expired.

Maintenance plans are available to maintain the 9100A/9105A at your site, to supplement the normal warranty period, or to do both. For specific information, contact your nearest Fluke Technical Service Center or Sales Representative.

Table 2-2. Required Tools and Test Equipment

EQUIPMENT REQUIRED FOR GENERAL SERVICING

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
Digital Multimeter	Fluke Model 77	
Oscilloscope	Philips Model PM 3065 (or equivalent)	
Adjustment Tool	P/N 800540	
Flat Blade Screwdriver		1/8-inch (3 mm) blade
Flat Blade Screwdriver		1/4-inch (6 mm) blade
Phillips Screwdriver		#2, blade 4 inches (10 cm) or longer
Hex Driver		3/16-inch (5 mm)
Hex Driver		5/16-inch (8 mm)
Wrench		3/16-inch (5 mm) or adjustable

REQUIRED EQUIPMENT FOR COMPONENT LEVEL REPAIR

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
9100A Service Kit	P/N 818948	
Digital Test Station, with I/O Module	Fluke Model 9105A (or 9100A) with 9100A-003 Option	Runs programs supplied with Service Kit
68000 Interface Pod	Fluke Model 9000A-68000	Used with Service Kit
Surface Mount Repair tools		See Table 4-6

Table 2-2. Required Tools and Test Equipment (cont.)

REQUIRED EQUIPMENT FOR MONOCHROME MONITOR MAINTENANCE

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
Hex Adjustment Tool	P/N 572321	Horizontal Size/Linearity
Alignment Template	P/N 777144	Use with Monitor Pattern Program
Long-Nose Pliers		
Flat-Blade Screwdriver		1/4-inch (6 mm) blade, plastic handle with blade at least 5 inches (12.5 cm) long.
Phillips Screwdriver		#2, plastic handle with blade at least 3 inches (7.5 cm) long.
Phillips Screwdriver		#2, non-magnetic tip blade, plastic handle, with blade at least 12 inches (30 cm) long, for crt replacement.
Torque Hex Driver		3/16-inch (5 mm).
Soft Pad (foam or quilted)		Approximately 8 x 10 inches (20 x 25 cm).
1 Megohm, 1W Resistor	P/N 109793	To discharge crt anode.
Clip Leads (2)		For connecting resistor to chassis and screwdriver shaft.
Safety Gloves		Mid-forearm length, soft leather.
Full Face Shield (preferred) or Safety Goggles		
Lab Smock with Zipper		Plastic zipper. Metal parts should not come in contact with the crt.

SPECIFICATIONS

Specifications for the 9100A/9105A are presented in Table 2-3.

Table 2-3. Specifications

ELECTRICAL SPECIFICATIONS

Probe

Input Threshold

Logic Level	TTL Voltage	CMOS Voltage	RS-232 Voltage
1	2.6 to 5.0V	3.7 to 5.0V	3.2 to 30V
1 or X	2.2 to 2.6V	3.3 to 3.7V	2.8 to 3.2V
X	1.0 to 2.2V	1.2 to 3.3V	-2.8 to 2.8V
X or 0	0.6 to 1.0V	0.8 to 1.2V	-3.2 to -2.8V
0	0.0 to 0.6V	0.0 to 0.8V	-30 to -3.2V

Input Impedance: 70 kilohm shunted by less than 33 pF

Data Timing for Synchronous Measurements

Maximum frequency	40 MHz
Minimum pulse width	
High or low	12.5 ns
3-state	20.0 ns
Setup times	
Data to Clock	5 ns
Start, Stop, or Enable to Clock	10 ns
Hold time	
Clock to Enable	10 ns
Clock to Start or Stop	0 ns

Data Timing for Asynchronous Measurements

Maximum frequency	40 MHz
Minimum pulse width	
High or low	12.5 ns
Invalid (X)	
TTL or CMOS	100 ns $\pm$20 ns
RS-232	2000 ns $\pm$400 ns

Table 2-3. Specifications (cont)

Transition Counting	
Maximum frequency	at least 40 MHz
Maximum count	16777215 (+overflow)
Maximum stop count	65535 clocks
Frequency Measurement	
Maximum frequency	at least 40 MHz
Resolution	20 Hz
Accuracy	±250 ppm ±20 Hz
Output Pulser	
High	>3.5V @200 mA for less than 10 us @ 1% duty cycle >4.0V @ 4 mA continuously
Low	<0.8V @ 200 mA for less than 10 us @ 1% duty cycle <0.4V @ 5 mA continuously
Clock Module	
Input Thresholds (all lines)	1.6V ±0.2V
Input Impedance	50 kilohm shunted by less than 10 pF
Clock, Start, Stop, and Enable Input Speed	
Maximum repetition rate	40 MHz
Minimum pulse width	12.5 ns

Table 2-3. Specifications (cont)

RS-232 Interfaces

One connector isolated (system-referenced), the other connector non-isolated (earth-referenced).

Baud rates	110, 134, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200
Parity	Odd, even, or none
Data bits	5, 6, 7, or 8
Stop bits	1, 1.5, or 2
XON/XOFF (Ctrl-S/Ctrl-Q)	Disable/Enable
Clear-to-Send	Disable/Enable
New line	Carriage Return and Line Feed (CRLF) or Carriage Return (CR)

I/O Module

Data Output

Current (>10 ms)	±200 mA ±10%
Current (<10 ms)	±2A ±10%
Pattern rate (one module driven)	Approximately 35 kHz
Pattern depth (one module driven during 10 ms high current pattern drive mode)	256 patterns
Maximum current (at Vout>=2V) (per pin, driving high)	275 mA
Maximum current (at Vout<=0.8V) (per pin, driving low)	150 mA

Table 2-3. Specifications (cont)

Input Thresholds

Logic Level	TTL Voltages	CMOS Voltages
1	2.6 to 5.0V	3.4 to 5.0V
1 or X	2.1 to 2.6V	2.9 to 3.4V
X	1.0 to 2.1V	1.2 to 2.9V
X or 0	0.6 to 1.0V	0.8 to 1.2V
0	0.0 to 0.6V	0.0 to 0.8V

Input Impedance — 50 kilohm minimum, shunted by less than 80 pF

Clock, Start, Stop, and Enable Inputs

Logic Thresholds
- Low — 0.8V maximum
- High — 2.0V minimum

Input Current — ±1 uA

Input/Output Overvoltage Protection

±15V for one minute maximum, any pin, one at a time

Transition Counting

- Maximum frequency — at least 10 MHz
- Maximum count (transition mode) — 8388607 counts (+overflow)
- Frequency accuracy (frequency mode) — ±250 ppm ±2 Hz

Stop Counter

- Maximum frequency — 10 MHz
- Maximum count — 65535 clocks

Clock

- Maximum frequency — 10 MHz
- Minimum pulse width — 50 ns

Table 2-3. Specifications (cont)

Data Timing for Synchronous Measurements

Maximum frequency of clock	10 MHz
Maximum frequency of data	5 MHz
Data setup time	30 ns
Data hold time	30 ns
Minimum pulse width (data)	75 ns
Minimum pulse width (Start, Stop, Enable, Clock)	50 ns
Start edge setup time (before clock edge, for clock edge to be recognized)	0 ns
Stop edge hold time (after clock edge, for clock edge to be recognized)	10 ns
Enable setup time (before clock edge, for clock edge to be recognized)	0 ns
Enable hold time (after clock edge, for clock edge to be recognized)	10 ns

Data Timing for Asynchronous Measurements

Maximum frequency	10 MHz
Minimum pulse width (high or low)	50 ns
Minimum pulse width (3-state)	150 ns

Data Compare Equal (DCE)

Minimum pulse width (Data and Enable)	75 ns

Table 2-3. Specifications (cont)

GENERAL SPECIFICATIONS

Line Voltage	90 to 132V ac, 47 to 440 Hz 180 to 264V ac, 47 to 63 Hz

Power Consumption

Mainframe	150W maximum
Monitor	50W maximum

Safety

Designed to meet ANSI/UL 478, IEC 348, IEC 435, and CSA 556B standards.

PHYSICAL SPECIFICATIONS

Operating Temperature

5° to 27°C, 95% RH maximum (noncondensing)

27° to 40°C, RH decreasing linearly from 95% to 50% (noncondensing)

Programmer's Station

24-line by 80-column crt monitor with video controller installed in mainframe. 87-key keyboard with separate cursor control, and hardkey and softkey function keys.

Storage/Shipping Temperature

-20° to 60°C, 8% to 80% RH (noncondensing). Micro-floppy media limited from 5° to 60°C, 8% to 80% RH (noncondensing).

Size

Mainframe	14.0 x 34.3 x 50.8 cm (H x W x D) (5.5 x 13.5 x 20.0 in)
Monitor	30.5 x 33.5 x 33.0 cm (H x W x D) (12.0 x 13.2 x 13.0 in)
ASCII Keyboard	5.1 x 21.2 x 47.2 cm (H x W x D) (2.0 x 8.3 x 18.6)

Weight

Mainframe	8.3 kg (18.2 lb)
Monitor	11.1 kg (24.5 lb)
ASCII Keyboard	1.6 kg (3.5 lb)

CONTENTS

OVERVIEW

This overview of the Fluke 9100A/9105A explains the general relationships of the unit blocks contained in the 9100A Block Diagram, Figure 3-1, and the 9105A Block Diagram, Figure 3-2. Wherever a block performs the same function for both instruments, an identical block name is used for ease of reference later in this section.

Main PCA

The Main Printed Circuit Assembly contains the following functional blocks:

- 68000 Microprocessor
- Read/Write (RAM) Memory
- Read-Only ROM Memory,
- Floppy Disk Drive Controller
- Pod Interface
- Power Supplies for the RS-232 ports, operator's display, and video.

The PCA contains the interfaces for expansion cards, serial ports, and the keyboards. There are connections for the Floppy Disk Drive, the Monitor, the Hard Disk Controller, the Probe I/O Module Interface, the microprocessor Pod, and the switching Power Supply.

RS-232 Ports

Two RS-232-C serial ports are available on the 9100A. These ports allow data transfer to and from the tester. One is system-referenced (isolated from earth) and is used with the UUT. The other is a non-isolated port and is used for connection to another tester, computer, or printer. The Serial Port connectors are located at the rear of the Chassis.

Micro Floppy Disk System

The Floppy Disk System uses 3.5-inch double-sided, double-density disks. A disk has a formatted capacity of 640K bytes. The 9100A uses one disk drive, and the 9105A uses two disk drives. The floppy drive is connected through J14 on the Main PCA.

Hard Disk System

The 9100A contains a 20M byte, 3.5-inch Hard Disk to store the operating software, user programs, and data. The Hard Disk interfaces to the Hard Disk Controller via the ST412 interface standard. The Hard Disk Controller interfaces to the Multi-Function Interface (MFI) PCA, which implements the SCSI interface standard. The MFI PCA, which plugs into the Main PCA at J6, also includes the battery-powered back-up clock for the 9100A.

Power Supply

The Power Supply for the 9100A/9105A is an OEM (original equipment manufacturer) switching power supply. Input voltage is switchable for either 90 to 132V ac or 180 to 264V ac operation. This functional block supplies one +5V, one -5V, and two +12V outputs to the system.

Operator's Display

The Operator's Display is a vacuum-fluorescent display, 254 pixels wide by 26 pixels deep, allowing for 42 characters per line. The Display is located above the Operator's Keypad on the Main Chassis. The Display Interface PCA is connected to J11 on the Main PCA.

Operator's Keypad

The Operator Keypad is a part of the Main Chassis unit that, when folded down, faces the operator. It is connected to J2 on the Display Interface PCA. It contains all of the keys needed by the operator to run pre-programmed tests used in the immediate troubleshooting mode.

Probe/Pulser

The Probe is a single-point, hand-held instrument that can measure signals up to 40 MHz. The Probe also acts as a pulser. The Probe is useful for portions of the board that cannot be accessed with the I/O Module or Pod. The Probe plugs into a connector on the side of the Chassis and is wired to J1 on the Probe I/O PCA.

Clock Module

The Clock Module is an external unit connected to the Main Chassis through J3 on the Probe I/O PCA. The Clock Module provides connections to external clock signals for troubleshooting signals asynchronous to the UUT microprocessor.

Monitor

The Monitor displays programming information entered from the Programmer's Keyboard. The Monitor can also assume Operator Keypad functions by displaying procedural information. The Monitor is connected to a Video Controller Card, which is plugged into the Main PCA.

Programmer's Keyboard

The Programmer's Keyboard is used for program development. It is also available as an option for data input to user programs. The Keyboard is connected to J10 on the Main PCA.

I/O Module

The I/O Module is an external unit used for data stimulus and response of up to 40 channels at one time. An assortment of clip modules is available for interface to the UUT. The 9100A can accommodate four I/O Modules at once, allowing for testing of 160 pins at a time. The 9100A has the capability to take CRCs (cyclic redundancy checks), measure frequency, take event counts, record logic levels, and drive output patterns on each pin. The I/O Modules plug into the I/O Connector PCA, which plugs into the Probe I/O PCA.

MAIN PCA (MC68000 MICROPROCESSOR)

Overview

The 9100A/9105A uses an MC68000 main processor(U32). The 16-bit MC68000 contains 17 32-bit registers, a 16-bit status register, and a 32-bit program counter. Of the 17 registers, 8 are data registers, 7 are address registers, and 2 registers are used as stack pointers. The MC68000 (U32) is located on the Main PCA of the mainframe.

The 68000 theory of operation covers the following:

- Signal and pin description
- Address/data operation
- Modes of processing including interrupts
- Asynchronous/synchronous execution
- Reset signal description and generation

Signal and Pin Description

The following paragraphs describe the meaning of each signal produced by the 68000 and show how these signals are organized per function. A table helps to explain the mnemonics used on the schematic, and indicates whether the signal is an input or an output. Figure 3-3 shows the 68000 pin configuration for the 68-pin plastic leaded chip carrier (PLCC) package.

SIGNAL DESCRIPTION

Table 3-1 describes the 68000 microprocessor signals.

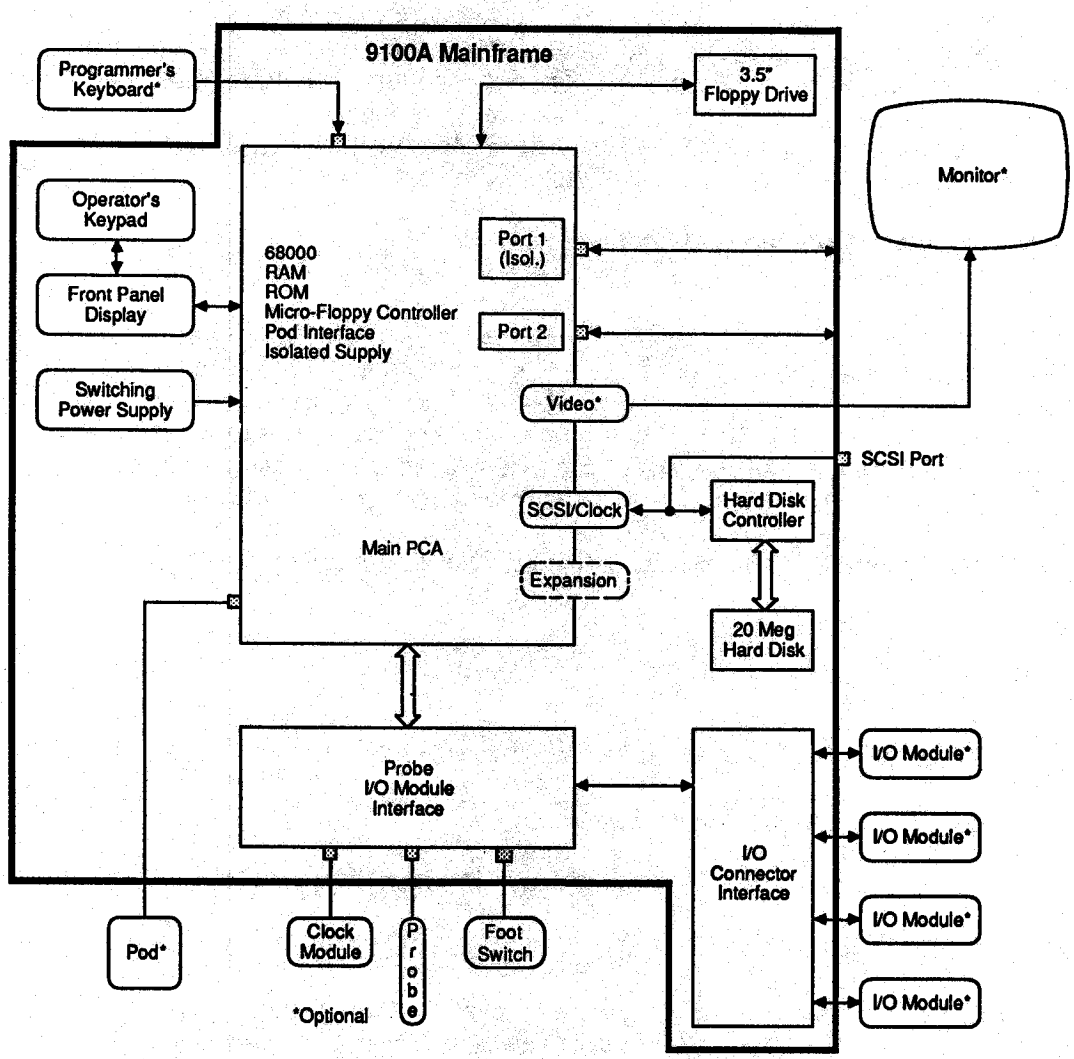


Figure 3-1. 9100A Block Diagram

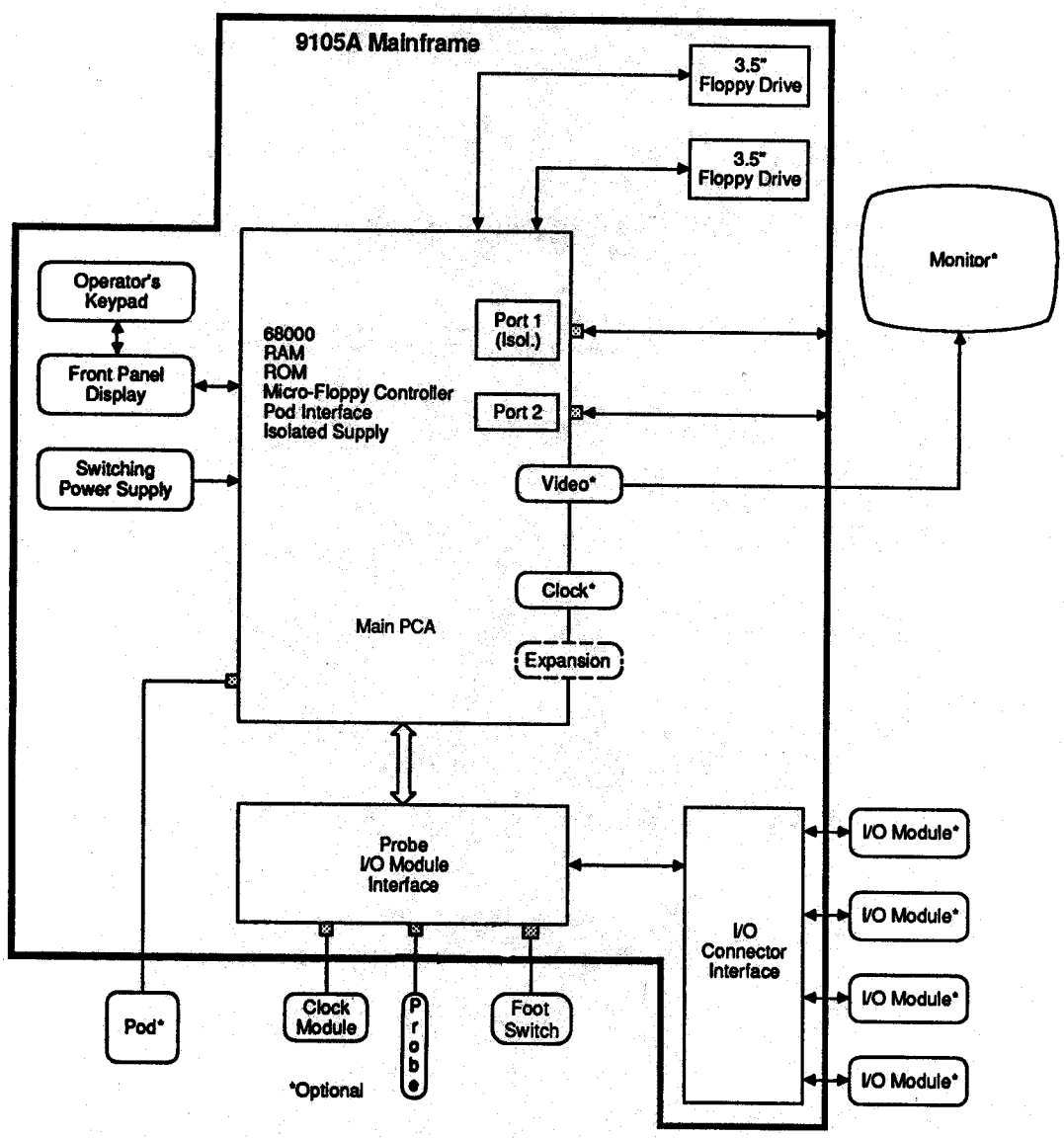


Figure 3-2. 9105A Block Diagram

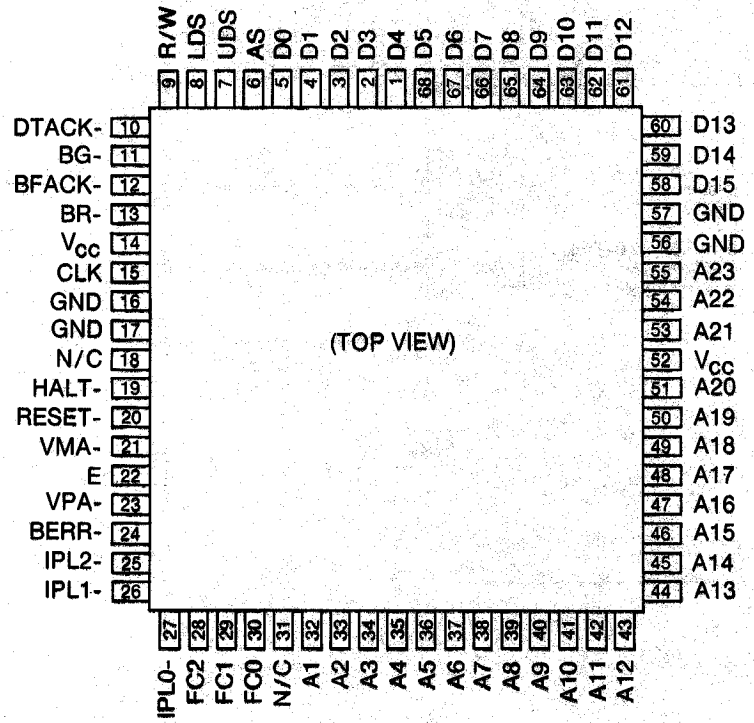


Figure 3-3. 68000 Pin Assignments

Table 3-1. Signal Descriptions

SIGNAL NAME	DESCRIPTION
A1 through A23	Address Bus: 23 tri-state output lines, providing the bus address for all processor operations except interrupt vector fetch cycles. During interrupt acknowledge cycles, address lines A1, A2, and A3 indicate the interrupt level that is being serviced, while address lines A4 through A23 are set high. Address line A0 is used internally by the processor for byte operations.
D0 through D15	Data Bus: 16-bit, bidirectional, tri-state data bus.
FC0 through FC2	Function Code lines: tri-state outputs that indicate the state (user or supervisor) and type (program or data) of the current bus cycle. They are also used to indicate an acknowledge cycle as follows:

FC2	FC1	FC0	CYCLE TYPE
0	0	0	(undefined, reserved)
0	0	1	User data
0	1	0	User program
0	1	1	(undefined, reserved)
1	0	0	(undefined, reserved)
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	Interrupt acknowledge

AS-	Address Strobe-: a tri-state output that indicates that valid data is present on the address and function code lines and that a bus cycle is in progress.
R/W-	Read/Write-: an output that indicates the direction that data is to be transferred on the data bus.
UDS-, LDS-	Upper Data Strobe- and Lower Data Strobe-: outputs that indicate whether upper, lower, or both bytes are to be used for a data bus transaction. During an interrupt acknowledge cycle, both UDS- and LDS- are asserted, but only the lower byte is read.
DTACK-	Data Transfer Acknowledge-: an input that indicates to the processor that the bus data transfer will be completed at the end of the current processor clock cycle. It is used to terminate the current bus cycle unless superseded by a bus error or a reset.
BR-	Bus Request-: an input that indicates to the processor that some other device is requesting control of the bus.

Table 3-1. Signal Descriptions (cont)

BG-	Bus Grant-: an output that indicates that the processor will relinquish control of the bus at the end of the current bus cycle.
BGACK-	Bus Grant Acknowledge-: an input that indicates that a device other than the processor has assumed bus control.
IPL0-, IPL1- IPL2-	Interrupt Priority Level-: inputs that indicate the encoded priority level of the interrupting device. Level 0 indicates no interrupt is pending, while level 7 is the highest priority interrupt.
BERR-	Bus Error Line: an input that indicates a problem with the current bus cycle. When BERR- is asserted with the HALT- line, the processor reruns the current bus cycle if the HALT- line is released first. If BERR- is asserted during reset vector acquisition, or for two consecutive bus cycles, the processor halts. If BERR- is asserted alone, it causes the processor to execute a non-maskable interrupt to the Bus Error Vector.
RESET-	Reset-: a bidirectional open collector line used to reset the state of the processor. It may also be used by the processor to reset the state of the external environment.
HALT-	Halt-: a bidirectional open collector line that is asserted when the processor stops due to an unrecoverable error sequence. This line can be pulled low during a bus cycle to stop the processor at the end of the cycle, to rerun the last bus cycle (when BERR- is low), or to reset the processor (when RESET- is low).
E	Enable: an output used to simulate a 6800-type processor clock for interface with 6800 family peripherals. This signal runs continuously and is derived by dividing the processor clock by ten. The duty cycle consists of six clock periods low and four clock periods high.
VPA-	Valid Peripheral Address: an input used to request 6800-type bus cycles. During interrupt acknowledge cycles, this line is used to request automatic vectoring.
VMA-	Valid Memory Address: an output used to enable 6800-type peripheral devices. VMA- indicates that the processor is synchronized to the Enable line and has placed a valid address on the address bus.
CLK	Clock: an input used to derive the clocks needed internally by the processor.

SIGNAL ORGANIZATION

The control signals of the 68000 can be grouped for the different functions. The function codes (FC0 through FC2) are the processor status signals that produce code sequences to indicate the mode (user or supervisor) and whether a data cycle or a program cycle is currently being executed. The code output is valid during an active address strobe (AS-). The code output is decoded externally to indicate interrupt acknowledge. The FC2 line is also used for address decode on the Multi-Function Interface PCA, the floppy controller chip, and the first 8K of RAM. This technique prevents user programs from accessing these areas.

The bus request (BR-), bus grant (BG-), and bus grant acknowledge (BGACK-) signals are used for bus arbitration control. These signals determine which component or peripheral controls the bus. The bus request input indicates that another device is requesting to become the bus master. The bus grant output then indicates to all other potential bus masters that the microprocessor will relinquish control at the end of this bus cycle. Once the other device has become the bus master, it returns the Bus Grant Acknowledge input to the microprocessor. These three bus arbitration control signals can be used by the Multi-Function Interface PCA to avoid bus contention.

Asynchronous bus control signals are Address Strobe (AS-), Read/Write (R/W-), Upper and Lower Data Strobes (UDS-, LDS-), and Data Transfer Acknowledge (DTACK-). The R/W- signal indicates the direction of data transfer on the data bus. When R/W- is high, data is being read from another functional block to the microprocessor. In the low state, data is being written to another functional block. The Upper and Lower Data Strobe signals are used in conjunction with the Read/Write signal to identify transfer of valid lower (D0 through D7) and/or upper (D8 through D15) data bytes. This data strobe control is defined in Table 3-2.

Table 3-2. Data Strobe Control

UDS-	LDS-	R/W-	UPPER D8-D15	LOWER D0-D7
High	High	-	none	none
Low	Low	Low	Write 8-15	Write 0-7
High	Low	Low	none	Write 0-7
Low	High	Low	Write 8-15	none
Low	Low	High	Read 8-15	Read 0-7
High	Low	High	none	Read 0-7
Low	High	High	Read 8-15	none

The Address Strobe (AS-) signifies that there is a valid address on the address bus. The Data Transfer Acknowledge (DTACK-) signal is an input signifying that data transfer is complete.

The System Control signals are Bus Error (BERR-), RESET-, and HALT-. The BERR- signal informs the microprocessor that there is a problem on the bus. The RESET- and HALT- signals reset or halt the 9100A/9105A system.

The 68000 uses three signal lines for peripheral control. The Enable (E), Valid Peripheral Address (VPA-), and Valid Memory Address (VMA-) allows for interfacing synchronous peripheral devices with the asynchronous 68000. The VPA- mode is not used in the 9100A/9105A system except for tests using the expansion connector on the Main PCA.

Address/Data Bus Operation

The address bus and the data bus are covered separately in the following discussion. For the address bus, size, contents, address ranges of the entire 9100A/9105A system are included. For the data bus, size and use are discussed.

ADDRESS BUS

The 23-bit address bus (A1 through A23) is used to access other functional blocks throughout the 9100A/9105A. If an interrupt occurs, address lines A1, A2, and A3 provide information about the type of interrupt, and the remaining lines are held high.

Table 3-3 shows ranges of memory available for various functional blocks. Actual addresses used within these ranges are defined under the appropriate functional block descriptions.

DATA BUS

The 16-bit data bus (D0 through D15) provides for bidirectional exchange of data between the microprocessor and an addressed functional block. Data lines D0 through D7 supply the vector number to the processor during an interrupt acknowledge cycle.

Bus Operation During Data Transfer

Three different types of cycles occur during data transfer: read, write, and read-modify-write. The following paragraphs explain the sequence of events during these cycles.

Table 3-3. Address Ranges

HEX ADDRESS	USE
000000 - 07FFFF	ROM
080000 - 08FFFF	Floppy Control *
090000 - 093FFF	DTIO #1: Keypad/Display, RS-232 Port #1 DTIO #2: ASCII Keyboard, RS-232 Port #2
094000 - 097FFF	Interrupt Vector (Read)
098000 - 09BFFF	Parity Error Latch (Read)
09C000 - 09FFFF	Pod Interface
0A0000 - 0AFFFF	Expansion Card Slot
0B0000 - 0BFFFF	Multi-Function Interface Card Slot
0C0000 - 0CFFFF	Logic Probe Circuitry
0D0000 - 0DFFFF	I/O Modules
0E0000 - 0EFFFF	Video RAM
0F0000 - 0FFFFF	Video Controller Chip
100000 - BFFFFF	unassigned
C00000 - FFFFFF	RAM **

* Supervisor Mode only
** C00000 - C01FFF accessible in Supervisor Mode only

THE READ CYCLE

The read cycle involves transmitting bytes of data from a peripheral or from a memory space to the 68000 processor. If a word is read, both the upper data strobe and lower data strobe are active. In the case of a byte operation, an internal A0 bit determines which byte to be read. The 68000 issues the required data strobe for that byte. When the lower data strobe (D00 through D07) is issued, the A0 bit equals 1; when the upper data strobe (D08 through D15) is issued, A0 equals 0.

THE WRITE CYCLE

The write cycle process involves the 68000 sending bytes of data to a peripheral or a memory location. As in the read cycle, the processor uses an internal A0 bit to determine if the high or low byte is written to, and the processor sends the required strobe signal. Both data strobes are active during a word write cycle.

THE READ-MODIFY-WRITE CYCLE

During the read-modify-write cycle, the 68000 performs a read, modifies the data internally, and writes the data to the original address. This cycle is used to let multiple processors communicate, and the address strobe is active throughout the cycle.

Bus Arbitration

The bus arbitration process is required to switch bus control from the 68000 to another device. First, the device sends a Bus Request Signal (BR-) to the microprocessor. The 68000 sends back a Bus Grant (BG-) signal at the end of the current bus cycle. To protect against noise interfering with bus arbitration, the microprocessor continues to process instructions when the BR- signal goes inactive and a BGACK- is not received. After receiving a BR- signal, the 68000 issues a BG- signal and an Address Strobe (AS-). The AS- signal indicates that a bus cycle is in progress. The BG- and AS- signals are not issued at the same moment; the BG- signal is delayed until the AS- signal is issued. When the device requesting the bus receives a BG-, the AS-, DTACK-, and BGACK- must be inactive before it sends a BGACK-. The device remains in control until it inactivates the BGACK- signal, which should be done only at the completion of the bus cycle(s).

A bus request can be initiated from any assembly attached to either the MFI or expansion connector, but not directly from the mainframe. The Main PCA does provide a priority encoding circuit that accepts a bus request (BR) and outputs a bus grant (BG). This circuit, composed of sections of U64 and U65, latches upon receipt of a bus request to ensure that the bus grant is output to the requesting device.

Bus Error and Halt

The 68000 transfers data asynchronously. That is, any device desiring to communicate with the microprocessor does so by handshake. If for some reason a handshake is not completed within seven microseconds, the hardware generates a Bus Error (BERR-) signal at U32-24. With BERR- active, the data and address busses are "off", and the current bus cycle is terminated. When the BERR- goes from active to inactive, several processes occur. The microprocessor stacks the contents of the program counter, the status register, and the error information. Next, a vector table address is read, and a software bus error handler routine from that address is then executed. Refer to Exception Processing later in this description for more information.

The BERR- acts similarly to a non-maskable interrupt, except that the microprocessor stores extra data on the stack. Bus errors can be used to detect the absence of accessories and options during initialization. The BERR- signal is generated by U40 using the enable (E) signal from J4.

The HALT- signal on U32-19 halts the microprocessor (after the current bus cycle) with a continuous active low. A continuous active high on this pin allows the 68000 to run.

If software tries to address a space with no valid memory, U40 asserts a bus error after six E clock periods. At any time, a write command to ROM also generates a bus error.

Privilege Modes

The following paragraphs explain activities of the 68000 that are not related to normal operation. The microprocessor exists in one of three modes: normal, exception, or halted. Exception processing and the 9100A/9105A system interrupts are covered. The normal situation allows for executing instructions, memory read and/or write, and storing results. A stop instruction stops the 68000 and is not related to a halt instruction.

Two types of privilege modes exist within the 68000: the supervisor mode and the user mode. The supervisor mode has higher priority than the user mode. The S-bit of the status register determines the mode in which the microprocessor operates. A 1 in the S-bit designates the supervisor mode, and all exception processing is performed in this state. All operations that require stacking during exception processing use the supervisor stack pointer.

The user mode is the lower of the two privilege modes, with 0 in the S-bit of the status register. Most instructions are executable (as in the supervisor mode) except for the stop and reset instructions. In the user mode the system stack pointer or address register 7 use the user stack pointer. To change from user to supervisor mode during the executing of instructions requires a change from normal to exception processing. To make this change the current status of the S-bit is saved, and the S-bit is forced to a 1. The set S-bit allows the microprocessor to resume the execution of instructions to process the exception in the supervisory mode.

Exception Processing

The 68000 categorizes resets, traps, interrupts, and bus errors as exceptions. Exceptions can be generated by either internal (software) or external (hardware) causes. All exceptions are assigned a number (0 through 255 decimal or 0 through FF hex). All exceptions are handled through a non-relocatable Exception Vector Table located at address 000000 through 0003FF. Each vector consists of four address bytes containing the exception handling routine address.

The externally generated exceptions are Reset, Bus Error, and Interrupt, all discussed in Table 3-1, Signal Descriptions. The internally generated exceptions can occur from program control operations such as trap (TRAP), trap on overflow (TRAPV), check data against upper bounds (CHK), divide (DIV), and trace (TRACE). In addition, software errors such as illegal instructions, word fetches from odd addresses, and privilege violations can cause exceptions. The internally generated exceptions act like non-maskable interrupts.

INTERRUPTS

The 9100A/9105A system uses 15 different interrupts allowing hardware and software to stop the 68000 operation and identify an error or specific condition. The interrupts are prioritized as follows according to their importance:

- The Parity Error Interrupt (I15) is level 7, which is non-maskable (NMI).
- All level 6 and lower levels are software maskable by level.
- Levels 7 through 2 are each used by only one interrupt.
- The level 1 interrupt is shared by several different interrupts. The interrupts within level 1 have priorities to prevent simultaneous requests.
- Level 0 indicates no interrupt is pending.

Pending interrupts are detected between instructions. An interrupt is acknowledged and the service routine started only if the pending interrupt has a higher priority than the current processor priority. When an interrupt is acknowledged, the hardware places a vector value on the data bus. This vector points to a memory location where the address of the interrupt routine is stored. Interrupts can be polled by reading the interrupt vector at byte location 094001. An interrupt request must be reset by the interrupt acknowledging routine. Individual interrupt descriptions in the following paragraphs provide more details.

A list of hardware generated exceptions and their vectors is shown in Table 3-4. These exception vectors are listed by priority with the top priority vector listed first. The maximum amount of vectors is 256. The vectors with priority levels 1 to 7 (refer to Table 3-4) are hardware generated at an interrupt acknowledge. Bus Error and Reset (Level *) behave differently; these exceptions always go to a predetermined address.

The interrupt circuitry located on the Main PCA contains two priority encoders (U49, U75), a D-type latch (U63), and several gates (U54B, U56A-D, U57A). This main interrupt system inputs each 9100A/9105A interrupt. When one interrupt or any number of interrupts go active low, U49 and U75 prioritize the interrupt to honor first. The highest priority interrupt is the Parity Error Interrupt, and the lowest priority is the Self-Vectored Interrupt. The correct priority is assigned to the interrupt control signals (IPL0, IPL1, and IPL2). When an interrupt acknowledge cycle occurs, U63 provides the correct interrupt vector to the data bus, and the reading produces a DTACK-. During a level 1 or self-vectored interrupt, U63 and the READINT- signal are disabled by EXT-INTA. An interrupt acknowledge is sent to the interrupting device through either the Multi-Function Interface PCA (MCINTA-) or the Expansion PCA (ECINTA-). The interrupting device can then supply the DTACK- and the vector.

Table 3-4. Interrupt Vector Table

Level	Number	Name	Hex Vector	Hex Address
*	RESET	Reset	00	00000
*	BERR	Bus Error	02	00008
7	I15	Parity Error Interrupt	8F	0023C
6	I14	Floppy Data Interrupt	9F	0027C
5	I13	DTIO # 1 Interrupt	AF	002BC
4	I12	DTIO # 2 Interrupt	BF	002FC
3	I11	MFI Card Interrupt 2	CF	0033C
2	I10	Expansion Card Interrupt 2	DF	0037C
1	I9	Floppy Control Interrupt	EF	003BC
-	I8	Not Usable	--	-----
1	I7	Probe Interrupt	78	001E0
1	I6	I/O Over Current Interrupt	79	001E4
1	I5	Pod Interrupt (see below)	7A	001E8
1	I4	Pod Power Fail Int (see below)	7B	001EC
1	I3	I/O Module General Interrupt	7C	001F0
1	I2	I/O Module DCE Interrupt	7D	001F4
1	I1	Video Controller Interrupt	7E	001F8
1	I0	Self-Vectored Interrupt	--	-----
-	--	No Interrupt	77	001DC

Interrupts and interrupt acknowledge for the MFI and expansion assemblies are handled in the same manner as bus requests and bus grants. Several sections of U64 and U65 provide a latch upon receipt of an interrupt to ensure that the first interrupting device receives the interrupt acknowledge.

Parity Error Interrupt

The 9100A/9105A checks parity on RAM reads. The 9100A/9105A tests high and low bytes separately. If the RAM read is a byte access, only the byte being read is tested. When a parity error is detected, the non-maskable Parity Error Interrupt (I15) is set, and microprocessor status information is latched. The latch is readable at address 098000 and is described in Table 3-5.

Table 3-5. Microprocessor Status Latches U61 & U62

BIT #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	FC1	PH	PL	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8

- FC1 is Function Control 1 from the microprocessor. It is low if the error occurred during a data access, and it is high if the error occurred during a program access.
- PH and PL are Parity High and Parity Low. One or both of these are set to indicate if the high or low byte of address had the error.
- A20 through A8 are the top bits of the address bus, allowing for error location within 256 bytes.

The latched information allows the processor to determine which 256-byte block of memory failed, whether the error was in the high or low byte, and if the failed location contained data or a program. When the processor reads this latch, the interrupt automatically clears.

Floppy Data Interrupt

The Floppy Data Interrupt is generated by the floppy controller either when it needs the next byte of data while doing a write or when the next byte of data is available in read mode. The interrupt is automatically cleared when the byte is received or read. The interrupt can be enabled or disabled by a bit in the floppy controller latch, and it can be individually polled at DTIO #2 Input Port, bit 4.

DTIO #1 Interrupt

The DTIO #1 Interrupt is generated by the DTIO (Dual UART/Timer/IO) #1 in response to a variety of conditions that may include the following:

- Transmit Buffer Empty
- Receive Buffer Full
- Break Received
- Timer Interrupt
- Pod Change
- 500 millisecond (Frequency Gate)

All possible interrupts can be polled at the ISR (Interrupt Status Register) of the DTIO. A separate register, the IMR (Interrupt Mask Register), is used to program which of the possible interrupts is allowed to generate an interrupt. After an interrupt is generated, the ISR must be read to determine the cause. Different actions are needed to reset the different types of interrupts.

DTIO #2 Interrupt

The DTIO #2 Interrupt is generated by the second DTIO and is similar in function to the DTIO #1 Interrupt. Possible DTIO #2 conditions include:

- Transmit Buffer Empty
- Receive Buffer Full
- Break Received
- Timer Interrupt
- Disk Change

MFI Card Interrupt 2

This interrupt is generated by a peripheral on a card plugged into the Multi-Function Interface (MFI) Card Slot. This interrupt is intended to be used by the SCSI controller chip under program control. This interrupt can be software disabled and polled instead. The MFI Card Interrupt is not used on the 9105A.

Expansion Card Interrupt 2

The Expansion Card Interrupt is reserved for devices connected to the expansion bus.

Floppy Controller Interrupt

The Floppy Controller Interrupt is generated by the floppy controller in response to a variety of conditions. The interrupt status register of the chip must first be read to determine the cause. This interrupt can be individually polled at DTIO #2 Input Port, bit 5.

Probe Interrupt

The Probe Interrupt is generated by the single-point probe for either a blown fuse or a button press. A probe chip status register read is performed to determine the cause.

I/O Overcurrent Interrupt

The I/O Module power supply generates an overcurrent interrupt, (IOOCI), when the current limit is exceeded. The interrupt is generated and latched on the Probe-I/O PCA, located in the mainframe. If this interrupt should occur, a control signal (ODRESET-) is sent to the I/O Module, which instantly turns off the overdrivers. Before clearing the interrupt, the overdrivers must be written to the tristate condition.

Pod Interrupt and Pod Power Fail Interrupt

The pod interrupts (I4, I5) are available and are polled, but they are not used by the 9100A/9105A.

I/O Module General Interrupt

This interrupt can be caused by a button press or a blown fuse on an I/O Module. The interrupt status register(s) on the I/O Module(s) must be read to determine the cause.

I/O Module Data Compare Equal Interrupt

The I/O Module Data Compare Equal Interrupt is generated by one of the I/O Modules when the programmed data compare register matches the input data. This interrupt can also be enabled to toggle MAINSTAT and/or ABORT to the pod. This allows DCE to cause the pod to exit quickly from RUNUUT or abort a test on a predetermined condition.

Video Controller Interrupt

The Video Controller Interrupt is reserved for use by the Video Controller PCA. The present pca does not use this interrupt.

Self-Vectored Interrupt

The Self-Vectored Interrupt (I0), is a special case. It can be generated by more than one device on either the MFI PCA Slot, or the Expansion Bus PCA Slot. A separate Interrupt Acknowledge (INTA) is sent to each pca slot to indicate which interrupt is being acknowledged. The initiating device must supply a vector and DTACK- or a VPA- (for auto-vectoring mode) when it is acknowledged.

No Interrupt

This vector is read if no interrupts are pending or if the interrupting device removed the request before the interrupt acknowledge cycle.

Asynchronous Execution

The 68000 can operate independently of the clock frequency by using only the handshake lines (AS-, UDS-, LDS-, DTACK-, BERR-, HALT-, and VPA-) for data transfer control. The AS- signal is issued by the microprocessor to begin the bus cycle. The data strobe signals verify that the data is valid on a write cycle. The memory space or peripheral places the requested data on the bus for a read cycle or latches the data on a write cycle. The DTACK- signal is issued by the data source to end the bus cycle.

If there is no response from the data source or if a wrong address is accessed, the BERR- or BERR- and HALT- are sent to the 68000 to abort or rerun the bus cycle. On a read cycle, the DTACK- signal can be sent before data is valid. A maximum of 90 nanoseconds is then available for valid data to be latched in the 68000. No maximum length of time is required between AS- and DTACK- signals.

Reset Signal Description and Generation

The following paragraphs describe the RESET- signal types, their use, and how they are produced on the Main PCA. The four types of resets are as follows:

- Power-Up Reset

  This is a "cold" start. It occurs at power up, allowing the processor to initialize the system.

- External Reset

  The hardware has an external switch that allows the user to reset the system. This reset button is debounced and shaped so it will not harm the RAM data. (The user probably was experiencing a situation that was abnormal to be using the reset button).

- Power Glitch Reset

  The mainframe has a special chip (U87) that detects the 5V dc supply falling below 4.5V dc. The length of the reset pulse is equal to the length of the power low time plus the time controlled by C12. If the power goes bad for a long time, the RAM data has probably been lost.

- Software Reset

  A Software Reset does not actually reset the microprocessor. Instead, it is a way for the software to toggle the RESET- line. A Software Reset can be used to reinitialize some peripherals such as the Floppy Disk Controller or the Application Keypad/VF Display Controller.

The reset circuitry located on the Main PCA contains a triggerable multivibrator (U88A), the external reset button (SW1), a power monitor (U87), two Schmidt trigger inverters (U71D, U71E) and a D-type flip-flop (U79A). The reset circuit contains a debounce circuit that cleans up the Ext-Reset signal once the user pushes SW1. U88A produces a long power up reset logic high signal during a cold startup, required by the 68000. The Power-Up Reset and Ext-Reset are gated by U78B to become the RESIN- input of U87. The U87 is used as a reset controller that supervises the supply voltage during power on. U87 keeps its output pin 5 active until the supply voltage reaches 5 volts. If the supply voltage drops below 4.7 volts, the circuit generates reset signals until 5 volts returns, to ensure a proper reset.

Address Decoding and DTACK

Address decoding for all circuits except RAM and ROM is accomplished by U17 and U70. U17 divides the low part of the address base into 64K segments. These segments are used by the floppy controller, the expansion bus connector, the multi-function interface, the probe, and the I/O Module. In addition, two segments are used by the video circuit. A final segment is further divided into 16K segments by U70. These segments are used by the UART (DTIO), interrupt logic, read parity control, and the pod.

Most address decode outputs connect to chip select inputs for the respective circuits. The DTACK- output, which instructs the microprocessor to complete the access cycle, is generated by U55 when the addressed circuit responds with the appropriate signal. For circuits requiring 0 wait states, the appropriate low signals are fed directly to U55. Other circuits require wait states to accommodate a longer access period. Parity reads, UART, and pod circuitry require one wait state. Video, floppy disk, and other pod circuits require three wait states. Signals for either number of wait states are fed through U34 and clocked into U55 by U50. U33 serves as an active pull-up for the DTACK signal out of U76.

Some peripherals require extra setup time during reads and writes. This requirement is satisfied with the new data strobe (NDS) signal from U79. During the write cycle, NDS is active one-half clock cycle after the address strobe. NDS is also withdrawn one-half clock cycle before the end of the write cycle to allow for data hold time.

RAM

RAM CONFIGURATION

Standard configuration includes 2M bytes of RAM for the 9100A and the 9105A. Either instrument can be expanded to 4M bytes of RAM. RAM is housed in single-in-line modules (SIMs), designated as U13, U14, U15, and U16. To achieve 2M bytes, four 512K-byte SIM modules are used. Memory expansion to 4M bytes can be achieved using four 1M-byte SIMs. The SIMs must be exchanged in pairs. The 9105A with serial numbers prior to 4352000 used a standard 1.5M-byte RAM configuration (two 512K and two 256K SIMs), expandable to 4M bytes as stated above.

An 8-segment DIP switch (U83) must be set for each RAM configuration. The settings are shown in Table 3-6. The RAM configuration is also saved as a code in non-volatile memory on the Main PCA (EEPROM U11).

Table 3-6. RAM Configuration (U83)

MODULE TYPE U13/U14	MODULE TYPE U15/U16	TOTAL BYTES	ADDRESS RANGE	SWITCH SEGMENTS 1234 5678
512K	256K	1.5M	C00000-D7FFFF	1001 1011 (9B)
512K	512K	2M	C00000-DFFFFF	1001 1001 (99)
1M		2M	C00000-DFFFFF	0010 0001 (21)
1M	1M	4M	C00000-FFFFFF	0011 0001 (31)
				1 = ON (closed)
				0 = OFF (open)

For each of these configurations, the first 8K bytes of RAM (C00000 through C01FFF) are accessible only by Supervisor Mode. An access to this area attempted by User Mode produces a Bus Error Exception and does not affect RAM contents.

RAM TIMING

To select a RAM address, U29, U30, and U31 multiplex 20 address lines (A01 through A20) into 10 address signals (RA0 through RA9). This multiplexed address is latched into RAM under control of both a row-address-strobe signal (RAS-) and a column-address-strobe signal (CAS-).

Upper (D15 through D08) and/or lower (D07 through D00) byte(s) can be read from bank 1 or 2. Bank 1 comprises U13 and U14. Bank 2 comprises U15 and U16. Clock signals and microprocessor read asynchronous bus control signals (LDS, UDS) determine read timing.

RAM REFRESH

RAM Refresh utilizes a state machine operating at approximately 33 kHz. RAM Refresh is initiated by a count of E clocks. E clocks are divided by two (U77B) and counted by U81. At every twelve E clocks, U81 generates refresh request (RFRQ). If there is no RAM access occurring at the same time, U85B generates refresh grant (RFGT). If a RAM access is occurring, RFGT is not generated until the end of the RAM access cycle. One-half cycle after RFGT, refresh address enable (RFAE) is generated to turn off the normal multiplexed address lines and enable the refresh address outputs from U26. One-half cycle later, U80A generates refresh RAS (RRAS), which performs the actual refresh. Refresh address is then disabled, and, through U68B, U81 is cleared. RFRQ and RFGT are thereby cleared. On each refresh, U85A changes states, clocking the refresh address output from U26. The Refresh cycle repeats 256 times in approximately 4 ms.

U85, pin 6 changes state for each refresh cycle. This transition is used as the lowest bit of the RAM refresh address through U33. On every change of the low bit, the clock to U26 is enabled to obtain the other eight bits of RAM refresh address (a nine-bit address).

Note that other uses of the U85 33 kHz signal include power supply switching and do not impact the scope of this discussion.

RAM PARITY

On every write cycle, parity is generated for each data byte. The high byte is generated by U24, and the low byte is generated by U23. The ninth bit into the parity comparator is held low during a write. If the parity on the rest of the bits is even, the EV (even) output of the parity comparator goes high. This output serves as a ninth bit of data, resulting in odd parity for the nine bits. If the parity on the rest of the bits is already odd, the ninth bit (EV) remains low to keep the parity odd.

On read cycles, this ninth bit serves as read data. Even parity at this time results in a parity error, which is latched for both high and low bytes by U73. U73 also outputs PLATCH (parity latch) to U61 and U62, latching the address and parity status bits. Parity interrupt is also generated at this time by U78. Refer to the Parity Interrupt description. The latches are cleared by either a reset or a read of the parity latches.

ROM

Sockets for U45/U48 (High Bank) and U46/U47 (Low Bank) accept 256K byte or 512K byte EPROMs, or 1M byte mask ROMs. A PAL (Programmable Array Logic), U28, provides four wire jumpers. Each jumper combination specifies select logic for the desired ROM configuration as shown in Table 3-7.

Table 3-7. ROM Select Logic

JUMPERS				SIZE	ADDRESSES	
W4	W3	W2	W1		Low Bank	High Bank
X	X	0	0	256K	00000 - 0FFFF	na
X	X	0	1	256K	00000 - 0FFFF	na
X	X	1	0	512K	00000 - 1FFFF	na
X	X	1	1	1M	00000 - 3FFFF	na
0	0	X	X	empty	na	none present
0	1	X	X	256K	na	40000 - 4FFFF
1	0	X	X	512K	na	40000 - 5FFFF
1	1	X	X	1M	na	40000 - 7FFFF

(0 = closed, 1 = open)

POD Interface

The Pod Interface accommodates information transfer in two bytes. A low byte is used as an 8-bit, bidirectional data port. U42 handles data (D00 through 07) inputs to the 9100A/9105A. Transparent latch U37 handles data outputs to the pod. An 8-bit, bidirectional high byte (status register) transfers information on data lines D08 through D15, using U58 for inputs and U53 for latched outputs.

Bit assignments for both status and data bytes are shown in Table 3-8. Latched outputs are cleared low by a reset.

Data or response from the Pod is read at handshake completion. Data from the 9100A/9105A to the Pod is latched when written. POD_OE must be active to enable the output buffer.

Refer to Table 3-9 for the pinout and function of each signal line for the Pod Interface.

On the 9100A, presence of a pod is indicated on the PODPRESENT- line when a valid signal is detected on the POWERFAIL line (J9-11).

Table 3-8. Pod Control Port Bit Assignment

STATUS BYTE (ADDRESS 9C000)

BIT	INPUT (U58)	LATCHED OUTPUT (U53)
D15	MAINSTAT	MAINSTAT
D14	POD_OE	POD_OE
D13	PODSTAT-	POD_RESET
D12	ABORT	ABORT
D11	PODPRESENT-	ENDCE-ABORT
D10	DCE	ENDCE-MAINSTAT
D09	PODINT	EN-PODINT
D08	POWERFAIL	EN-PWRINT

NAME	I/O	DESCRIPTION
MAINSTAT	I/O	Handshake line from 9100A/9105A to the Pod.
POD_OE	I/O	Enables the Pod data buffer for write data. A high true signal enables (drives) the latched output data onto the Pod data lines (POD0 through POD7).
POD_RESET	O	Signal from 9100A/9105A to reset the Pod.
ABORT	O	Signal from the 9100A/9105A telling the Pod to abort a long operation.

Table 3-8. Pod Control Port Bit Assignment (cont)

ENDCE-ABORT	O	Enables the I/O Module Data Compare Equal (DCE) Signal to set the ABORT signal to the Pod. This allows the Pod to abort an operation upon a preprogrammed condition.
ENDCE-MAINSTAT	O	Enables the I/O Module Data Compare Equal (DCE) signal to set the MAINSTAT signal to the Pod. This allows the Pod to abort a RUN UUT upon a preprogrammed condition or address.
EN-PODINT	O	Enables the PODINT Signal from the Pod to interrupt the processor.
EN-PWRINT	O	Enables the POWERFAIL Signal from the Pod to interrupt the processor.
PODSTAT-	I	Active low handshake line from Pod.
PODPRESENT-	I	A low true signal that indicates when a Pod is connected to the Pod Interface connector. This signal is derived from the Pod interface POWERFAIL signal. This signal can be enabled to generate an interrupt through the DTIO on change of state, (i.e., connecting or disconnecting the Pod).
DCE	I	Monitors the I/O Module Data Compare Equal (DCE) Signal.
PODINT	I	Buffered active high interrupt line from certain pods. This line will also generate an interrupt if enabled by EN-PODINT.
POWERFAIL	I	Active when Pod detects a bad UUT power supply. Can be enabled to cause an interrupt if EN-PWRINT is set.

DATA BYTE (ADDRESS 9C001)

BIT	INPUT (U42)	LATCHED OUTPUT (U37)
D07-D00	READ DATA	WRITE DATA

Table 3-9. Pod Interface Pinout

NAME	FUNCTION	PIN
POD0	Data bit 0	8
POD1	Data bit 1	20
POD2	Data bit 2	7
POD3	Data bit 3	19
POD4	Data bit 4	6
POD5	Data bit 5	18
POD6	Data bit 6	5
POD7	Data bit 7	17
MAINSTAT-	Handshake	12
PODSTAT-	Handshake	24
PODRESET-	Resets Pod	23
POWERFAIL	Power out of tolerance	11
PODINT-	Pod interrupt	1
ABORT-	abort	9
PODSYNC-	Pod Sync	10
SYNC SH	Pod sync shield	22
+5V	+5 volt power	2,15
+12V	+12 volt power	14
-5V	-5 volt power	21
GND	Ground	4,13,16,25
X SHLD	Pod cable shield	3

DUART-Timer-I/O

The 9100A/9105A uses two 2681 DTIOs (U12 as DTIO1 and U7 as DTIO2). Each performs multiple Dual Asynchronous Receiver/Transmitters (DUART), timers, and input/output functions with two serial ports, one parallel input port, one parallel output port, and a timer.

For DTIO1, register addressing and descriptions are given in Table 3-10. Specific functions are:

- Programmable Timer Interrupt
  - OP3: timer output (50 ms)
  - INT-: Interrupt Request to microprocessor

- EEPROM Control
  - IP4: data output from EEPROM
  - OP4: data input to EEPROM
  - OP5: serial clock to EEPROM
  - OP6: chip enable to EEPROM

- Pod Present Detection
  - IP2: PODPRESENT change-of-state detection (can generate interrupt)

- Frequency Gate Generation/Detection
  - IP3: FGATE frequency gate input
  - OP2: frequency gate load

- DTIO1, Serial Port A: Application Keypad/Display
  - TxDA: Data to Application Keypad/Display
  - RxDA: Data from Application Keypad/Display
  - CTSA- (IP0): Clear to Send from Application Keypad/Display.

  Transmit and receive are at 19.2K baud. This port automatically holds off transmission data when the Keypad/Display is too busy to accept data.

- DTIO1, Serial Port B: Earth Referenced RS-232 Port #2
  - TxDB: Transmit Data
  - RxDB: Receive Data
  - CTSB- (IP1): Clear to Send
  - RTSB- (OP1): Request to Send

  Supports programmable baud rates, data width, stop bits, parity, and interrupts on buffer conditions, with three-deep FIFO on both transmit and receive.

For DTI02, register addressing and descriptions are provided in Table 3-11. Specific functions are:

- DTI02, Serial Port A: Programmers Keyboard
  RxDA: Programmers Keyboard Data

  The baud rate is 1200 baud. The keyboard has a separate reset line, which is connected to OP7 of DTI0 #2.

- DTI02, Serial Port B: System Referenced RS-232 Port #1
  TxDB: Transmit Data
  RxDB: Receive Data
  CTSB- (IP1): Clear to Send
  RTSB- (OP1): Request to Send

  Supports programmable baud rates, data width, stop bits, parity, and interrupts on buffer conditions, with three-deep FIFO on both transmit and receive.

- Second Programmable Timer Interrupt
  OP3: Timer output, Divide by 16
  INT-: Interrupt Request to microprocessor

- Floppy Disk Change Detection
  IP2: Drive 1 Disk Change (can generate interrupt)
  IP3: Drive 2 Disk Change (can generate interrupt)

- Floppy Disk Interrupt Monitor
  IP4: Read Floppy Drive Data Interrupt Bit
  IP5: Read Floppy Drive Interrupt Bit

- Programmers Keyboard Reset
  OP7: KBRST- Keyboard Reset

- I/O Module Power Supply Control
  OP5: I/O Module Reset
  OP6: I/O Module Low Current
  IP6: Input from I/O or Probe Board (spare)

- Other
  OP2: RUN UUT LED Drive
  OP4: Disk Access LED Drive

Table 3-10. DTIO #1 (Channels A, B)
Register Addressing and Description

MSA	$90001	* mode register channel A (R/W)
SRA	$90003	* status register channel A (R)
CSRA	$90003	* clock select register A (W)
CRA	$90005	* command register A (W)
ADATA	$90007	* data holding registers A (R/W)
IPCR	$90009	* input port change register (R)
ACR	$90009	* aux control register (W)
ISR	$9000B	* interrupt status register (R)
IMR	$9000B	* interrupt mask register (W)
CTU	$9000D	* counter/timer upper data (R)
CTL	$9000F	* counter/timer lower data (R)
CTUR	$9000D	* counter/timer upper register (W)
CTLR	$9000F	* counter/timer lower register (W)
MRB	$90011	* mode register channel B (R/W)
SRB	$90013	* status register channel B (R)
CSRB	$90013	* clock select register B (W)
CRB	$90015	* command register B (W)
BDATA	$90017	* data holding registers B (R/W)
INP	$9001B	* input port (R)
OPCR	$9001B	* output port configuration register (W)
SCC	$9001D	* start counter command (R)
SOPB	$9001D	* set output port bits command (W)
STC	$9001F	* stop counter command (R)
ROPB	$9001F	* reset output port bits command (W)

Table 3-11. DTIO #2 (Channels C, D)
Register Addressing and Description

MRC	$90000	* mode register channel C (R/W)
SRC	$90002	* status register channel C (R)
CSRC	$90002	* clock select register C (W)
CRC	$90004	* command register C (W)
CDATA	$90006	* data holding registers C (R/W)
IPCR	$90008	* input port change register (R)
ACR	$90008	* aux control register (W)
ISR	$9000A	* interrupt status register (R)
IMR	$9000A	* interrupt mask register (W)
CTU	$9000C	* counter/timer upper data (R)
CTL	$9000E	* counter/timer lower data (R)
CTUR	$9000C	* counter/timer upper register (W)
CTLR	$9000E	* counter/timer lower register (W)
MRD	$90010	* mode register channel D (R/W)
SRD	$90012	* status register channel D (R)
CSRD	$90012	* clock select register D (W)
CRD	$90014	* command register D (W)
DDATA	$90016	* data holding registers D (R/W)
INP	$9001A	* input port (R)
OPCR	$9001A	* output port configuration register (W)
SCC	$9001C	* start counter command (R)
SOPB	$9001C	* set output port bits command (W)
STC	$9001E	* stop counter command (R)
ROPB	$9001E	* reset output port bits command (W)

MICROFLOPPY DISK SYSTEM

Disk Drive

The 9100A uses one OEM 3.5-inch, double-sided, double-density microfloppy disk drive. On the 9105A, two of these drives are used. Each disk uses 80 tracks per side (0 to 4F hex), formatted as 16 sectors of 256 bytes per track, for a formatted capacity of 640K bytes. Each drive is accessed and formatted through the Floppy Controller.

Floppy Drive Controller

An FD1797 floppy controller (U43) and an FDC9229 Floppy Disk Interface Circuit (FDIC) are used for floppy drive control. The floppy controller does not format the floppy disk; this function is performed through software. The controller does perform the following functions:

- It searches for the correct track and sector.
- It calculates CRC values and inserts all required CRC's during a write.
- It serializes data on a write and decodes data on a read.

The FDIC circuit (U44) performs digital data separation and track-selectable write pre-compensation.

Addresses for U43 Floppy Controller registers are shown in Table 3-12.

Table 3-12. Floppy Controller Addressing

NAME	ADDRESS	DESCRIPTION
DCOMND	$80001	* Disk Command Register (write)
DSTAT	$80001	* Disk Status Register (read)
DTRACK	$80003	* Disk Track Register (read/write)
DSECTOR	$80005	* Disk Sector Register (read/write)
DDATA	$80007	* Disk Data Register (read/write)

Output latch U60 (address 80000) controls drive selects and other features. Table 3-13 describes U60 outputs.

Table 3-13. Floppy Drive Control Latch Outputs

NAME	DESCRIPTION
DS0, DS1	Drive Selects (turn on motor and enable communications with floppy controller for one drive at a time.)
SPARE	(not used)
MINI	Controls Floppy Controller clock to select data rate for mini (5 1/4- or 3 1/2-inch, logic low) or standard (8-inch, logic high) drive.
DENS	Selects between single density (logic low) and standard double density (logic high).
P0, P1	Selects the write pre-compensation time, as shown below.

P1	P0	TIME
0	0	0 ns
0	1	125 ns
1	0	250 ns
1	1	375 ns

EN-INT: Enables the floppy data interrupt.

Interrupts

The Floppy Data Interrupt is generated by the floppy controller when it needs the next byte of data while doing a write or when the next byte of data is available in read mode. The Floppy Data Interrupt is automatically cleared when the byte is received or read.

The Floppy Controller Interrupt is generated by the floppy controller in response to a variety of conditions. The chip's interrupt status register must first be read to determine the cause. This interrupt can be polled at DTIO #2 Input Port, bit 5.

HARD DISK SYSTEM

On the 9100A, a standard-feature, O.E.M.-supplied hard disk occupies the space otherwise used in the 9105A for a second floppy disk drive. System software that is resident on this 20M byte, 3.5-inch hard disk is backed up with floppy disks.

The hard disk controller, also an O.E.M. product, attaches to the Internal SCSI Connector (J2) on the Multi-Function Interface (MFI) PCA, which is plugged into J6 on the Main PCA.

POWER SUPPLY

An OEM switching power supply is used to operate from a line voltage of 90 to 132V ac (47-440 Hz) or 180 to 264V ac (47-63 Hz). Single outputs of +5.1V dc and -5V dc and two outputs of +12V dc are provided. The 9100A power supply is rated at 150W (maximum). Pin designations for the power supply are presented in Table 3-14.

Table 3-14. Power Supply Pinout

DC OUT			AC IN	
TB1-1	+12V	4.0 Amps +/- 5%	TB2-1	AC Hot
-2	+12V	2.0 Amps +/- 10%	-2	AC Neutral
-3	-5V	1.0 Amp +/- 5%		
-4,5,6	Power supply common		-3	AC Earth ground
-7,8	+5.1V	15.0 Amps +/- 4%		

OPERATOR'S DISPLAY

Vacuum-Fluorescent Display (VFD)

The vacuum-fluorescent display uses a 254 by 26 pixel layout. Each character comprises a six wide by eight deep group of pixels, allowing for a total width of 42 characters per line (numbered 0 through 41). A pseudo-character at position 42 allows for a backspace to effect character 41. The cursor cannot be positioned prior to character 0 or after character 42. The display contains up to four lines (numbered 0 through 3).

A total depth of 26 pixels allows for display of either three lines separated with a blank row (character mode), or three full lines and a partial fourth line (graphics mode). The character mode is the default at startup.

The vacuum fluorescent display is in essence a tube, with the filaments forming a heated cathode. A switcher circuit supplies 12V to one side of the filament and about 4V to the other side. These voltages are switched at the end of each scan cycle (after all grids have been scanned). The switching is synchronized to the scan rate to prevent flicker.

Each switching cycle is controlled by U14 and its associated output drivers. Two discrete actions occur at the start of each cycle. The filament drive is first switched off briefly. Next, the filament is driven (through Q2/Q6 or Q3/Q5) in the direction opposite to that used in the last cycle. Transistors Q2 and Q6 are used during one cycle direction, and Q3 and Q5 are used during the other cycle direction. U31 supports the filament drive switch off function.

The vacuum fluorescent tube grids are driven in pairs. Grid input (GI) is held high for two clock periods at the beginning of the refresh cycle. The grid drivers are shift registers that are clocked to the next set of grids with each refresh scan. The grids are driven in pairs, G1 and G2, followed by G2 and G3, and so on. This scheme is illustrated in Figure 3-4.

Anodes comprise rows A1 through D24, which are also driven in pairs. Rows A and B (or C and D) are enabled together. If dots associated with only one row are on, both rows in the pair are still enabled.

The Z8 display processor, U1, both receives inputs, data, and commands from the main microprocessor and sends data out through a TTL-level RS-232 interface. Divider U4 uses the Y1 reference clock signal (fed through U1) to derive timing signals for the circuit. U1 uses multiplexed address timing for data output; U2 latches the address for use with RAM and shift registers.

U1 receives the code for the character to be displayed, converts the code to the appropriate pixel pattern, and then writes the converted code to the appropriate row and column of the display RAM. However, U1's main function is to refresh the display tube. U1 uses pointers to the grid counters, reads data from display RAM, and, by holding A11 high, simultaneously writes data to serial shift registers U23 and U24. The state machines U14B and U15B shift the data out of the U23/U24 parallel-serial converters into the correct row drivers. This process is repeated four times for each refresh, at which time the data is latched into the row drivers.

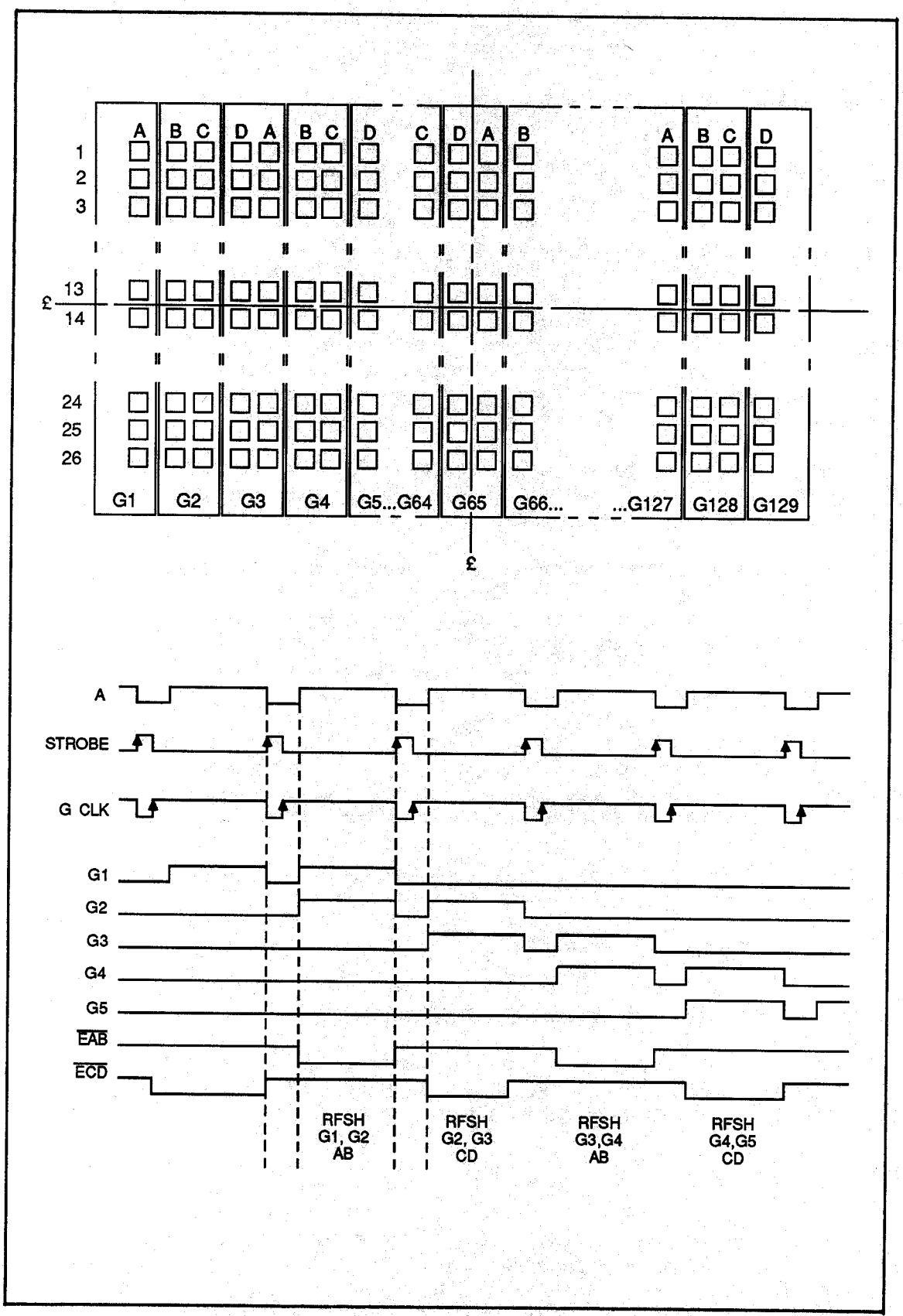


Figure 3-4. Vacuum Fluorescent Display

The SET- pulse from U1 provides the master timing signal for this refresh process. When SET- is true, grid input (GI) is also true. U13 and U14 provide the 1/4-3/4 duty cycle signal A, which is the master timing signal. One A cycle corresponds to one grid pair refresh. STROBE is used to strobe data into the row drivers. GCLK (the inverse of STROBE) is used to clock the grid drivers to the next position (G1/G2 to G2/G3, etc.). Row driver enable is provided by EAB- (for rows A and B) and by EAD- (for rows C and D). Outputs to display grid and row drivers incorporate pull-up resistors to provide valid MOS voltage levels. All grid and row drivers are disabled at reset or power-up by DSPYE (display enable) from U25.

Both grid and row currents flow through the filaments. Therefore, after a reset, the processor, U1, clears all grids and rows before a new enable is output. This action prevents filament destruction due to excess current.

Auxiliary circuitry includes the LED drivers. The RUN UUT and DISK ACCESS LEDs are driven by the Main PCA; all other LEDs are controlled by U1 (with latch U30) on the Display Interface PCA.

At the end of each display refresh, the processor scans the keypad by writing to U26, a 4-to-1 decoder. U26 drives one of the column lines low. The processor then reads the ROWBUSS to determine if any row line has been pulled low, signifying a keypress. Only one key press at a time is recognized by the processor. That key press must be withdrawn before another can be recognized. Multiple key presses are not recognized.

U28 is a shift counter whose output is used for character or graphics mode. In the character mode, nine bits are shifted out (the ninth bit designates a blank between text lines). This cycle is repeated three times, and five bits are shifted out on the fourth cycle to yield the 32 bits. In the graphics mode, an eight-bit load/shift-out cycle is repeated four times to derive 32 bits.

U29 provides a free-running oscillator for the beeper. The processor can enable either or both of two tones.

Resets are handled by U18 and U31, which reset the processor, clear all latched LEDs through U30, and clear all outputs of U25.

A 20-wire ribbon cable connects the Operator Display and Keypad to a Main PCA serial port. Data is exchanged at 19.2K baud. Ribbon cable connections are described in Table 3-15.

Displayable Characters

The characters shown in Table 3-16 (hex values 20 through FF) are displayable. Some of the display characters are not available through TL/1 programs, but can be accessed by the Main PCA processor using the hex values listed. The character codes shown in Table 3-17 are control codes of the display. These codes, which do not represent displayable characters, perform certain control functions.

Table 3-15. Ribbon Cable Connections

LINE	USE	TYPE	DESCRIPTION
10,12,14,20	Ground		
16,18	12 Volts	Power	Power for filament and for bell
6,8	5 Volts	Power	Power for logic
4	70 Volts	Power	Power for vacuum fluorescent display
1,5	Earth		Green Ground
19	Key		Key for alignment
17	RESET	Input	Active high resets the processor
15	TRANSMIT	Output	Transmits data to Main PCA at 19.2K baud
13	RECEIVE	Input	Receives data from Main PCA at 19.2K baud
11	CTS-	Output	Active low holds off Main PCA transmit
9	ROW7	Input	Last row of the keypad scan
7	COLUMN9	Output	Last column of the keypad scan
3	RUN-LED	Input	Controls "RUN UUT" LED
2	DISK-LED	Input	Controls "DISK ACCESS" LED

Table 3-16. Display Characters

20 = ' '	30 = '0'	40 = '@'	50 = 'P'	60 = '`'	70 = 'p'
21 = '!'	31 = '1'	41 = 'A'	51 = 'Q'	61 = 'a'	71 = 'q'
22 = '"'	32 = '2'	42 = 'B'	52 = 'R'	62 = 'b'	72 = 'r'
23 = '#'	33 = '3'	43 = 'C'	53 = 'S'	63 = 'c'	73 = 's'
24 = '$'	34 = '4'	44 = 'D'	54 = 'T'	64 = 'd'	74 = 't'
25 = '%'	35 = '5'	45 = 'E'	55 = 'U'	65 = 'e'	75 = 'u'
26 = '&'	36 = '6'	46 = 'F'	56 = 'V'	66 = 'f'	76 = 'v'
27 = '''	37 = '7'	47 = 'G'	57 = 'W'	67 = 'g'	77 = 'w'
28 = '('	38 = '8'	48 = 'H'	58 = 'X'	68 = 'h'	78 = 'x'
29 = ')'	39 = '9'	49 = 'I'	59 = 'Y'	69 = 'i'	79 = 'y'
2A = '*'	3A = ':'	4A = 'J'	5A = 'Z'	6A = 'j'	7A = 'z'
2B = '+'	3B = ';'	4B = 'K'	5B = '['	6B = 'k'	7B = '{'
2C = ','	3C = '<'	4C = 'L'	5C = '\'	6C = 'l'	7C = '|'
2D = '-'	3D = '='	4D = 'M'	5D = ']'	6D = 'm'	7D = '}'
2E = '.'	3E = '>'	4E = 'N'	5E = '^'	6E = 'n'	7E = '~'
2F = '/'	3F = '?'	4F = 'O'	5F = '_'	6F = 'o'	7F = Full Block

80 = reduced '0' (upper left)	88 = reduced '8' (upper left)
81 = reduced '1' (upper left)	89 = reduced '9' (upper left)
82 = reduced '2' (upper left)	8A = bracket (lower right)
83 = reduced '3' (upper left)	8B = bi-directional pin
84 = reduced '4' (upper left)	8C = large pin above chip
85 = reduced '5' (upper left)	8D = I.C. pin above chip
86 = reduced '6' (upper left)	8E = up arrow
87 = reduced '7' (upper left)	8F = down arrow
90 = reduced '0' (lower right)	98 = reduced '8' (lower right)
91 = reduced '1' (lower right)	99 = reduced '9' (lower right)
92 = reduced '2' (lower right)	9A = bracket (upper left)
93 = reduced '3' (lower right)	9B = omega
94 = reduced '4' (lower right)	9C = large pin below chip
95 = reduced '5' (lower right)	9D = I.C. pin below chip
96 = reduced '6' (lower right)	9E = left arrow
97 = reduced '7' (lower right)	9F = right arrow

Table 3-16. Display Characters (cont)

A0 = reduced '0' (center)	A8 = reduced '8' (center)
A1 = reduced '1' (center)	A9 = reduced '9' (center)
A2 = reduced '2' (center)	AA = divide sign
A3 = reduced '3' (center)	AB = +/-
A4 = reduced '4' (center)	AC = micro
A5 = reduced '5' (center)	AD = inverted '-'
A6 = reduced '6' (center)	AE = pi
A7 = reduced '7' (center)	AF = pound sign
B0 = reduced inverted '0' (center)	B8 = reduced inverted '8' (center)
B1 = reduced inverted '1' (center)	B9 = reduced inverted '9' (center)
B2 = reduced inverted '2' (center)	BA = I.C. head
B3 = reduced inverted '3' (center)	BB = I.C. body segment (full splat)
B4 = reduced inverted '4' (center)	BC = reduced splat (center)
B5 = reduced inverted '5' (center)	BD = box
B6 = reduced inverted '6' (center)	BE = double box
B7 = reduced inverted '7' (center)	BF = super-reduced splat
C0 = boxed super-reduced splat	C8 = reduced inverted 'H'
C1 = reduced inverted 'A'	C9 = reduced inverted 'I'
C2 = reduced inverted 'B'	CA = reduced inverted 'J'
C3 = reduced inverted 'C'	CB = reduced inverted 'K'
C4 = reduced inverted 'D'	CC = reduced inverted 'L'
C5 = reduced inverted 'E'	CD = reduced inverted 'M'
C6 = reduced inverted 'F'	CE = reduced inverted 'N'
C7 = reduced inverted 'G'	CF = reduced inverted 'O'
D0 = reduced inverted 'P'	D8 = reduced inverted 'X'
D1 = reduced inverted 'Q'	D9 = reduced inverted 'Y'
D2 = reduced inverted 'R'	DA = reduced inverted 'Z'
D3 = reduced inverted 'S'	DB = logic 1 level
D4 = reduced inverted 'T'	DC = logic x level
D5 = reduced inverted 'U'	DD = logic 0 level
D6 = reduced inverted 'V'	DE = 0 -> 1 edge
D7 = reduced inverted 'W'	DF = 0 -> x edge
E0 = x -> 1 edge	E8 = reduced inverted *
E1 = 1 -> 0 edge	E9 = reduced inverted up arrow
E2 = 1 -> x edge	EA = reduced inverted down arrow
E3 = x -> 0 edge	EB = not yet defined
E4 = left inverse line	EC = not yet defined
E5 = left line	ED = not yet defined
E6 = right inverse line	EE = not yet defined
E7 = right line	EF = not yet defined
F0 through FF = not yet defined	

Two control modes are available. The first, display mode, specifies display of the two bit maps (page 1 or page 2) as follows:

- o Display Mode 0 — Alternately displays Page 1 and Page 2 at a fixed rate of approximately 1 Hz. Display mode 0 is the default at startup.
- o Display Mode 1 — Displays Page 1 only
- o Display Mode 2 — Displays Page 2 only

The second, write mode, controls placement of the character as follows:

- o Write Mode 0 — Places the character in both Page 1 and Page 2. Write mode 0 is the default.
- o Write Mode 1 — Places the character in Page 1 only.
- o Write Mode 2 — Places the character in Page 2 only.

Table 3-17. Control Characters

HEX	FUNCTION	DESCRIPTION
00	Load bell	Load bell value
01	Time out	Set time out value
02	no op	(not used)
03	Blink	Blank location in page 2, advance cursor, and set write mode 0.
04	Flash	Put the complement of the character at the page 1 cursor into page 2, advance cursor, and set write mode 0.
05	Character mode	Place extra blank dot between lines
06	Graphics mode	No extra blank dot between lines
07	Bell	Ring bell
08	Cursor left	Move cursor one character left
09	Cursor right	Move cursor one character right
0A	Cursor down	Move cursor one line down
0B	Cursor up	Move cursor one line up
0C	Clear	Place in display mode 0, place in write mode 0, clear entire display, and home cursor
0D	<cr>	Carriage return
0E	Test	Perform tests on hardware
0F	Move cursor	Move cursor to a new location
10	<bs>	Backspace and delete
11	Annunciators	Turn annunciators on or off
12	Blink mask	Make annunciators solid or blink
13	XOR next char	XOR with display the next character and advance cursor
14	Clear to eol	Clear to end of line
15	Clear line	Clear entire line and place cursor at zero character
16	Invert next char	Invert the video of the character and advance cursor

Table 3-17. Control Characters (cont.)

17	Underline	Underline character at the cursor and advance cursor
18	Display mode 0	Set display mode 0
19	Display mode 1	Set display mode 1
1A	Display mode 2	Set display mode 2
1B	Graphics	Next 6 bytes define the graphics to be placed in the display
1C	XOR graphics	Next 6 bytes define the graphics to be XORed with the old display value
1D	Write mode 0	Set write mode 0
1E	Write mode 1	Set write mode 1
1F	Write mode 2	Set write mode 2

Annunciators

Seven LED annunciators are used with the display: BUSY, STOPPED, RUN UUT, STORING SEQ, DISK ACCESS, MORE SOFTKEYS, MORE INFORMATION. The RUN UUT and DISK ACCESS LEDs are controlled by the Main PCA; the other LEDs are controlled by the Display PCA.

OPERATOR'S KEYPAD

The 55-key keypad consists of 50 hard-labeled keys and five soft-labeled keys. An LED annunciator, located on the keypad, lights when the alpha mode is activated. Functionally, the keypad is a 9-column by 8-row matrix. Pressing a key completes a connection between a particular column output and row input.

The keypad is scanned by the Display PCA after every display refresh. If a new key closure is detected at this time, the appropriate byte is sent via the serial output to the Main PCA. Values returned for each key are shown in Table 3-18.

A tenth column output (COLUMN9) is not used on the keypad. COLUMN9 is routed (along with the ROW7 input signal) across the Main PCA to the Probe I/O PCA. This arrangement allows for scanning the external footswitch input. A closure of the footswitch connection is detected and the appropriate byte sent to the Main PCA in the same fashion as with a key closure on the keypad.

PROBE I/O MODULE INTERFACE

Overview

The Probe I/O Interface provides the interface from the mainframe to the single-point Probe, Clock Module, and the I/O Connector PCA. The Interface PCA is mounted flush to the Main PCA inside the mainframe. The Probe I/O Interface block diagram, Figure 3-5, contains the following functional block groups:

- o Address Decoding
- o Probe Interface
- o Clock Module Interface
- o Custom Delay Probe Chip
- o Custom Probe Logic Chip
- o Stop Counter
- o I/O Module Interface
- o Miscellaneous Functional Blocks

Table 3-18. Key Values

KEY	VALUE	ASCII	KEY	VALUE	ASCII
SOFTKEYS	58	X	B (1011)	42	B
F1	59	Y	SETUP MENU (P)	24	$
F2	5A	Z	SEQ (Q)	25	%
F3	5B	[	POD (R)	2C	,
F4	5C	\	ROM (S)	2D	-
F5	5D	]	STIM (T)	34	4
RESET	5E	^	4 (0100)	35	5
ALPHA	20	space	5 (0101)	3C	<
EXEC (G)	21	!	6 (0110)	3D	=
PROBE (H)	28	(	7 (0111)	44	D
BUS (I)	29	)	(up arrow)	4C	L
READ (J)	30	0	REPEAT (-)	54	T
C (1100)	31	1	STOP	55	U
D (1101)	38	8	OPTION (U)	26	&
E (1110)	39	9	(V)	27	'
F (1111)	40	@	SYNC (W)	2E	.
ENTER YES	41	A	(X)	2F	/
CLEAR NO	48	H	RUN UUT (Y)	36	6
EDIT (.)	50	P	0 (0000)	37	7
HELP	51	Q	1 (0001)	3E	>
MAIN MENU (K)	22	"	2 (0010)	3F	?
GFI (L)	23	#	3 (0011)	46	F
IO MOD (M)	2A	*	←	47	G
RAM (N)	2B	+	(down arrow)	4E	N
WRITE (O)	32	2	→	4F	O
8 (1000)	33	3	LOOP (Z)	56	V
9 (1001)	3A	:	CONT (SPACE)	57	W
A (1010)	3B	;	footswitch	6F	o

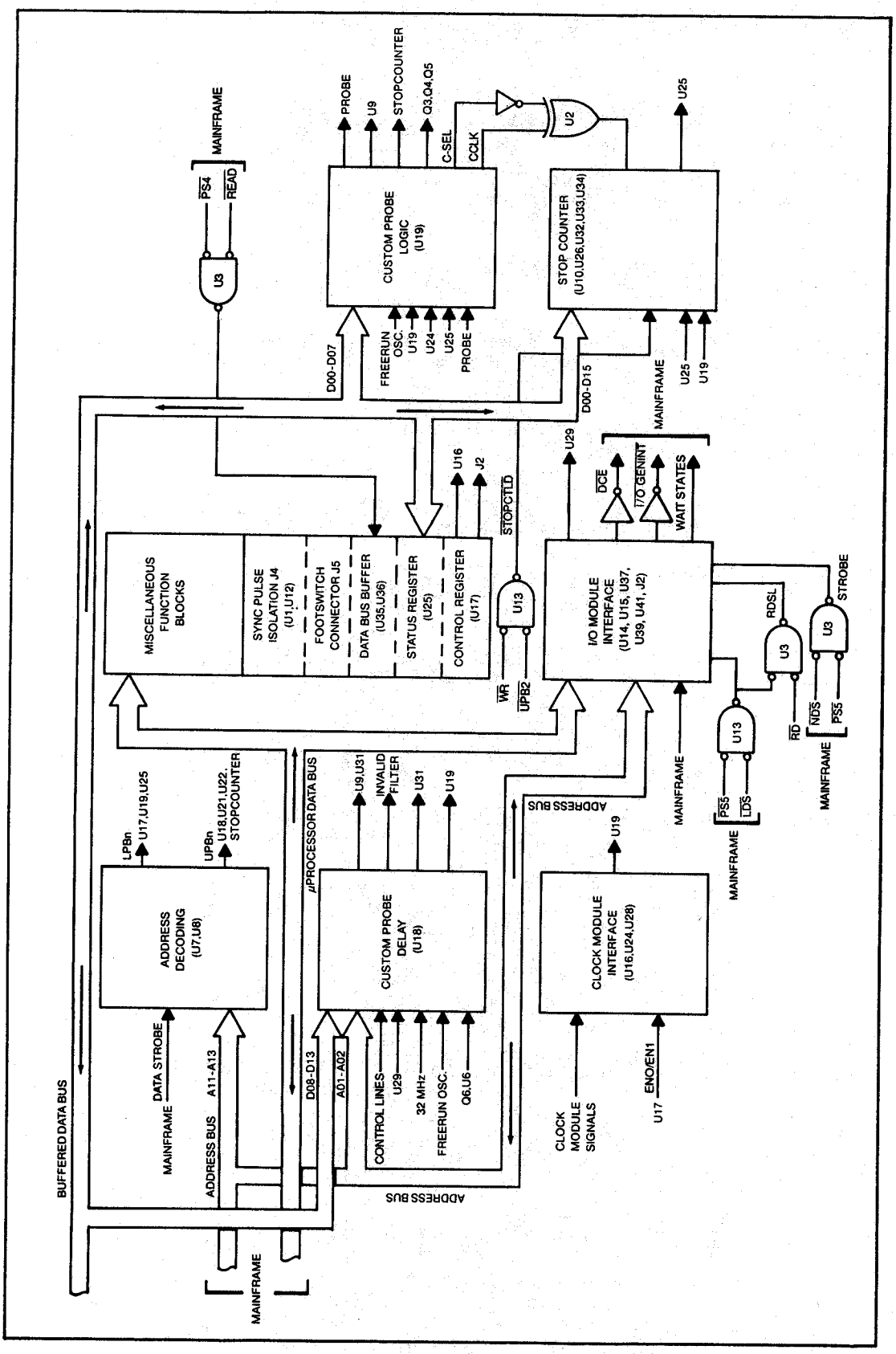


Figure 3-5. Probe I/O Interface Block Diagram

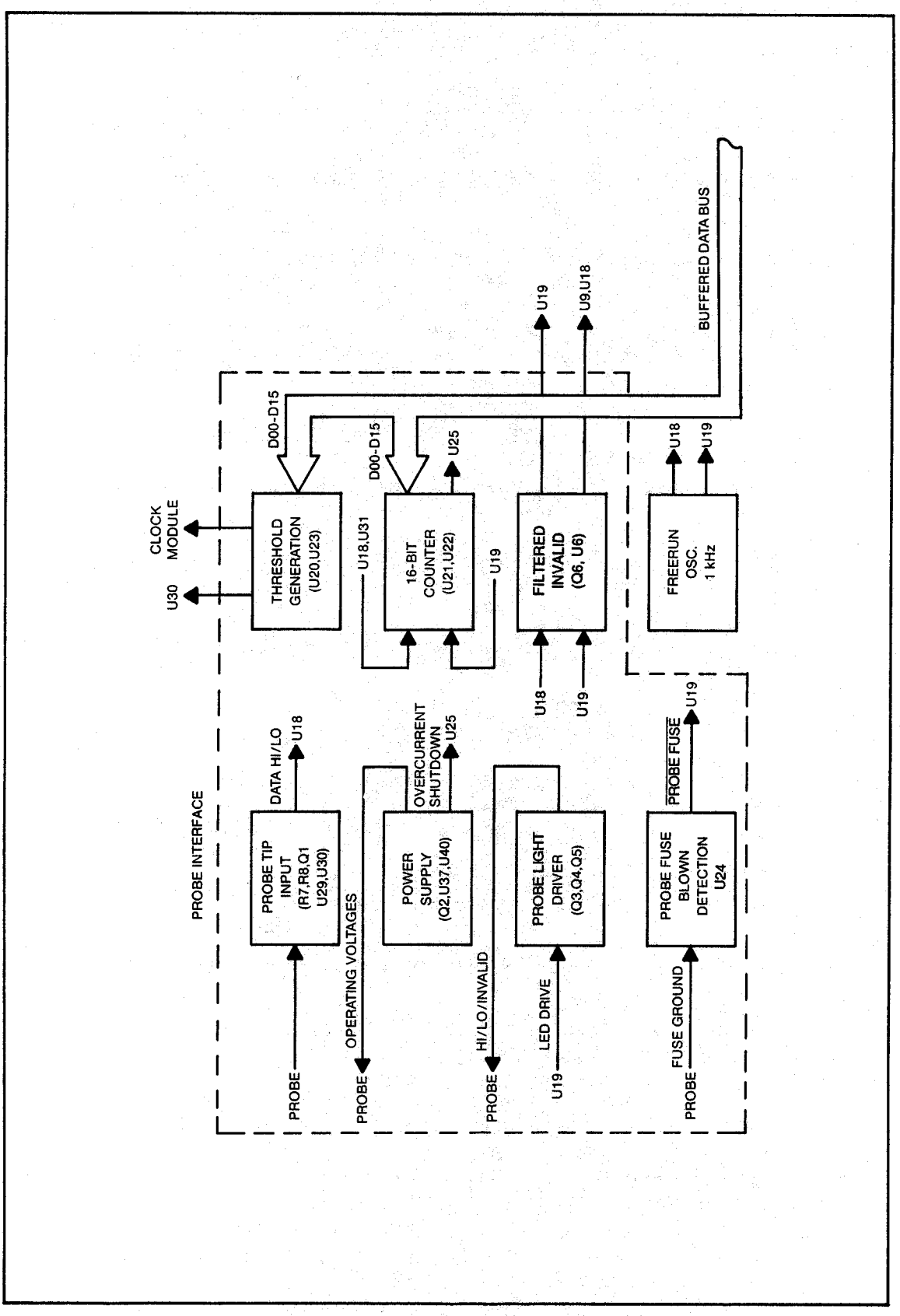


Figure 3-5. Probe I/O Interface Block Diagram (cont)

Probe I/O Module Interface Addressing

The 9100A/9105A allocates two 64K blocks of address space for the Probe and I/O Module system. The address space for the Probe, 0C0000 through 0CFFFF, is selected by PS4- (Peripheral Select 4). The four strobe signals PS4-, UDS- (Upper Data Strobe), LDS- (Lower Data Strobe), and NDS- (New Data Strobe) are gated by NAND gates (U7) to produce an active low enable input for each of the two 1-of-4 Decoder/Demultiplexers (U8). Address bits A11 and A12 are used as the address inputs to U8 to produce Upper and Lower Probe Bank chip select signals. The Upper Probe Bank contains address locations for U18 internal registers, high threshold D/A converter (U23), Stop Counter data and the Pulse Counter (U21, U22). The Lower Probe Bank contains address locations for the Probe Custom Logic chip internal registers, low threshold D/A converter (U20), control register (U17), and the status register (U25). The address map for the Probe I/O Module Interface is located in Table 3-19.

Table 3-19. Probe I/O Module Interface Address Map

ADDRESS	WIDTH	COMPONENT	R/W-
C000x-	(even bytes) (0 through 6)	Probe Delay Chip	(Read/Write)
C000x	(odd bytes) (1 through F)	Probe Logic Chip	(Read/Write)
C0800	(byte)	High Threshold D/A Converter	(Write)
C0801	(byte)	Low Threshold D/A	(Write)
C1000	(word)	External Stop Counter	(Write)
C1001	(byte)	Status Register	(Read)
C1800	(word)	16-bit External Counter	(Read)
C1800	(byte)	Clear External Counter and Delay Chip Latched Registers	(Write)
C1801	(byte)	Control Register	(Write)

Probe Interface

The Probe Interface group block in Figure 3-5 contains smaller specific blocks that contain circuitry for the following:

- Controlling data input by the Probe.
- Generating voltages used by the Probe.
- Controlling and driving the Probe lights.
- Detecting blown probe fuse.
- Counting frequency, transitions, or periods with bit counters.

PROBE DATA INPUT

The signal from the Probe tip passes through a resistor divider network on the single-point Probe PCA and the Probe I/O Module PCA. A FET (Q1) buffers the signal before high-speed dual comparator U30 samples the signal. The comparator thresholds are set by programmable digital-to-analog converters (DACs) U20 and U23. The low DAC (U20) generates the low threshold by receiving input data on D00 through D07 from the buffered data bus; the high DAC (U23) generates the high threshold from D08 through D15 of the same bus. The probe data input threshold voltages can be set in 10 millivolt increments by the DACs. The outputs of U30 are converted from ECL (Emitter-Couple Logic) levels to TTL levels before entering the Custom Gate Array Delay Chip (U18).

If the Probe I/O PCA is repaired or replaced, a probe offset calibration is required. This calibration value is stored in an EEPROM on the Main PCA. Any offsets in the FET (Q1) are corrected by adding the calibration value to the U20 and U23 voltage.

THRESHOLD VOLTAGE CALCULATION

The following paragraphs describe how voltages on the Probe I/O PCA and Probe PCA determine the input voltages to U30 and output voltages of U20 and U23. The calculated results aid the technician in determining if the pca components are operating properly. The example below determines U30 output and U20 and U23 input voltages.

STEP 1: Calculation of U20 and U23 multiplier.

A. Attenuation from probe input to U30.
   a = R8/(R8 + RSERIES) = 15K/(15K + 100370) = .130
   RSERIES = probe series resistance

B. Attenuation from U20 and U23 to U30
   b = R51/(R51 + R50) = 511/(511 + 1150) = .307

C. a/b = .130/.307 = .42

STEP 2: Calculation of U20 and U23 output voltage. (TTL level)

LOGIC LEVEL	REAL THRESHOLD VOLTAGE		U20 AND U23 OUTPUT VOLTAGE
Hi	2.4V	* .42 =	1.00V
Lo	2.8V	* .42 =	0.33V

STEP 3: Calculation of U30 input voltage.

LOGIC LEVEL	U20 AND U23 OUTPUT VOLTAGE		U30 INPUT VOLTAGE
Hi	1.00V	* .307 =	.307V
Lo	.33V	* .307 =	.101V

Three choices of probe input threshold are available to the user: TTL, CMOS, and RS-232. To generate a negative threshold from U20 in RS-232 applications, the software sets a bit in the probe custom logic chip (U19) to set the RS-232- signal active. This signal is used to force a negative 3.2 volt threshold on U20. Various voltage threshold levels are presented in Table 3-20.

Table 3-20. Voltage Threshold Levels

TARGET VOLTAGES		REAL THRESHOLD VOLTAGE	DAC OUTPUT VOLTAGE	U30 INPUT VOLTAGE
	TTL			
5.0V	----------			
	Guaranteed HIGH			
2.6V	-----			
	high or invalid	2.4 volts	1.0 volt	.31 volt
2.2V	-----			
	Guaranteed INVALID			
1.0V	-----			
	low or invalid	0.8 volt	0.33 volt	.10 volt
0.6V	-----			
	Guaranteed LOW			
0.0V	----------			
	CMOS			
5.0V	----------			
	Guaranteed HIGH			
3.7V	-----			
	high or invalid	3.5 volts	1.47 volts	.45 volt
3.3V	-----			
	Guaranteed INVALID			
1.2V	-----			
	low or invalid	1.0 volt	0.42 volt	.13 volt
0.8V	-----			
	Guaranteed LOW			
0.0V	----------			
	RS-232			
30V	----------			
	Guaranteed HIGH			
3.2V	-----			
	high or invalid	3.0 volts	1.26 volts	0.39 volt
2.8V	-----			
	Guaranteed INVALID			
-2.8V	-----			
	low or invalid	-3.0 volts	0	-0.39 volt*
-3.2V	-----			
	Guaranteed LOW			
-30V	----------			

* Pulled negative by Q8 and R60.

PROBE OPERATION VOLTAGES

Two voltage levels (regulated +5 volts and -1.2 volts) are produced on the Probe I/O Interface PCA. The +5 volts is used for the Pulse High probe signal and as power for U1. The +12VN (nonregulated) voltage is converted to +5 volts by a +5 volt regulator (U40). Voltage comparator U37 acts as an overcurrent shutdown sensor for the +5 volt supply. A -1.2 volt power supply (Q2) converts -5 volts to -1.2 volts used to produce Pulse Low for the Probe.

FUSE BLOWN DETECTION

Fuse blown detection circuitry for the Probe is located between the probe connector and the Probe Custom Chip. The probe ground fuse (F1), located on the Probe I/O Interface, protects circuitry in case the user incorrectly connects the ground clip to a power supply. Detection for blown fuses is generated by two LM339 voltage comparators (U24) that generate the output Fuse-P.

PROBE LIGHT DRIVE AND CONTROL

The Probe Light Control block contains a 2:1 Line Multiplexer (U9), and a 4-bit Data Latch (U31). The 2:1 Line Multiplexer selects latched/unlatched data. Invalid asynchronous data is filtered by the Filtered Invalid block, which requires that the invalid signal persist for 100 ns before being detected. Synchronous data invalid levels are taken as is on the clock edge. The output of the Filter block is multiplexed with the invalid signal from U31 to become INVALID IN at U19-58 along with the High and Low outputs of U9. The HI IN, INV IN, and LO IN pulses are stretched 50 ms internally within U19 to to become the light drive inputs to Q3, Q4, and Q5.

The three transistors Q3, Q4, and Q5 drive the three logic level indicator lights on the Probe. Each transistor drives one light:

- Q3 for the (green) low logic level light.
- Q4 for the (yellow) invalid logic level light.
- Q5 for the (red) high logic level light.

The input signals to the transistors originate from U19-28, U19-29, and U19-30.

EXTERNAL 16-BIT COUNTER

Two 8-bit binary counters (U21, U22) are cascaded together to form a 16-bit external counter. The 16-bit counter together with a 8-bit internal counter of U19 combine into a 24-bit counter. The 24-bit counter counts transition changes, clock frequency counts, and period counts from data collected by the probe tip.

Clock Module Interface

The Clock Module Interface on the Probe I/O Module Interface PCA contains a Quad ECL-TTL Translator (U28), a Dual 4:1 Line Multiplexer (U16), and a fuse blown detection circuit. The START/START-, STOP/STOP-, ENABLE/ENABLE-, and EXT CLK/EXT CLK- signal lines are ECL (Emitter-Coupled Logic) level outputs of the Clock Module. These outputs are converted to TTL level signals before being introduced to U19. Before entering U19, the ENABLE/ENABLE-, SYNC, EN1, and ENO signals are combined to form a multiplexed input line to U19-24 via U16 for the purpose of selecting an External Enable. A blown Clock Module fuse detection circuit signals to the mainframe that a Clock Module fuse is blown. Two voltage comparators (U24) detect the blown fuse and generate the blown fuse signal (FUSE-C) to U19.

Custom Delay Chip

The Custom Delay Chip (U18) is one of two Probe Control chips on the Probe I/O Module Interface PCA. The functional block located on Figure 3-5 contains internal components dealing with Probe Input Signal Delay. The function of U18 is to produce high, low, and invalid data signals including CRC data and CRC clock generation. These signals are sent to support chips and to the Custom Probe Logic Chip (U19).

The Delay Chip contains a data multiplexer that can select either the Probe threshold or a presently unused current input U18-5. A FREERUN signal (a 1-kHz continuous square wave) and a input clock is used for internal calibration. The CURRENT input is for future expansion purposes. Once data is past the multiplexer, two separate data paths form the DATA HIGH, the DATA LOW, and INVALID OUT outputs. The Enable Clock U18-19 has a 60 ns delay switchable in or out (0 delay or 60 ns delay). A history and CRC data latch contained in U18 provides valid data (high or low) or the last valid data input for the CRC register in U19.

Functions of U18 include:

- Delaying data high and low from the probe tip input for U31 and U9 to interpret.
- Latching synchronous/asynchronous Hi, Lo, and Invalid Probe Data.
- Generating CRC clock and CRC data signals used by U19 from Enable Clock input.
- Generating INVOUT signal output at U18-34.
- Qualifying CRC Clock Data, either present data or last valid data.

An Invalid signal, which amounts to a lack of valid high or valid low, is generated by the custom delay chip as the INVOUT signal. This is routed through a filter (U6 and associated resistor/diode arrays); the resulting output is termed Filtered Invalid. In asynchronous mode, the invalid pulse must exceed 100 ns in width. This is accomplished by using

an RC network to delay the trip point of U6, pin 1 by 100 ns. An invalid input exceeding 100 ns trips this circuit, producing the filtered invalid output. In asynchronous mode, this output is used by both the internal latches and the probe light circuitry. For the RS-232 threshold, Q6 is used to switch in C34, increasing the RC timing and producing a longer filter time of about 2000 ns for the invalid signal. The RS-232- signal from U19 is also used to pull the U20 logic level negative through level shifters Q7 and Q8.

Synchronous invalid constitutes an absence of a valid low or valid high at the clock time.

For accurate probe operation, the delays in the probe system must be calibrated. Before delay calibration can be performed, the software must determine the amount of delay per tap on the delay line internal to the custom delay chip (U18). At power-up or reset, an external 32 MHz clock signal is routed through both the high and low data paths. By choosing differing amounts of delay and counting clock edges, the software is able to compute the amount of delay per internal delay line tap. This data is saved for use in delay calibration.

The clock delay (60 ns) is switched in for negative delays, and the data delay is switched in for positive delays. Calibration is accomplished by adding delays and reading the pca's history latches. Note that any change in the external lights during this process results from pulses being fed through related circuits and has no other significance.

The delay calibration value is computed by the probe calibration procedure. Both the Clock Module and the Probe are used during the procedure, with the Probe tip being pulsed to generate the calibrating clock signal. Delays are adjusted until both the clock (probe tip pulse) and the data arrive at the history latch at the same time. The delay value derived is saved in memory and can then be stored on disk for subsequent use.

Custom Logic Chip

The second of two custom chips on the Probe I/O Module, the Probe Custom Chip, is located on the functional block diagram Figure 3-5. Internal structure and the functions of U19 deal with Probe Data signals, Probe Light drive, counting events, and clock selection. The Custom Logic chip contains the following internal structures:

- Digital Pulse stretcher circuitry for Probe Lights.
- A counter configurable for frequency, period, or transition.
- Pulser control logic.
- A CRC register circuit.
- Start_stop_enable logic for the clock.
- A multiplexer to select the clock.

The Custom Logic Chip supports functions from both the Probe and the Clock Module with different clock-type selection (Pod SYNC, FREERUN, and EXT CLK) determined within U19. CRC data is also calculated by U19.

Predetermined synchronous or asynchronous data selected by the 2:1 Line Multiplexer (U9) on the Hi in, Invalid in, and Lo in signal lines are stretched by U19 to at least 50 ms. The stretched signals become the three light drives for Q3, Q4, Q5.

An 8-bit internal counter (U19) and a 16-bit external counter (U21, U22) perform three counting modes: transition, frequency, and period. These functions count either data high transitions or 8 MHz clock transitions and are controlled as described below:

- Transition Mode: The counter counts data transitions with a software controlled start/stop.

- Frequency Mode: The counter counts the data transitions for a 50-ms period. The software converts this count to frequency by multiplying the count by 20.

- Period Mode: The counter counts the 8-MHz clock from one data high transition to another. The software uses this mode to measure low frequencies, converting the count from period to frequency for display.

CRC data is gathered at the internal CRC register (part of U19). The CRC uses the delayed data and clock signals from U18.

PULSE HI and LO signals for the Probe are generated by U19 to stimulate signal lines in the UUT. To produce pulser signals, a logic low from an internal clock logic register plus a Hi, Lo, or software- generated clock enter a pulse logic register. The two outputs of the pulse logic register are the PHI and PLO signals on U19, pins 10 and 26, respectively.

The Probe Logic Chip contains an internal selection system to provide the enabled clock for U18 and the 16-bit Stop Counter, and to provide a SYNC Pulse to an externally-connected oscilloscope via a BNC connector located on the mainframe back panel. EXT START and EXT STOP from the Clock Module, and STOPCNT- are combined to enable the internal clock signal input to the internal Clock Logic Register of U19. The selected enable, SYNC-, FREERUN, and EXT CLOCK from the Clock Module combine to enable the internal Clock Logic Register, which generates the enabled clock outputs CCLK and CCLK-.

When the probe/pulser is active, the internal clock logic requires the opposite edge of the pulse to start the clock; in a non-pulsing condition, the clock starts on the first selected edge to provide an edge (before the clock edge) to start the probe output pulse. The clock is inverted internally in U19 when the pulser is active. The CSEL output is high when the clock has been inverted internally, forcing pins 3 and 6 of U2 to invert the clock outputs again to provide the correct signals to U18 and the sync output.

Stop Counter

The Stop Counter is a series of four presettable 4-bit binary up/down counters (U26, U32, U33, U34). Each counter has four parallel data inputs to count the total 16 data bus lines. STOPCTCK (Stop Count Clock) from U2-6 is the clock pulse for the counter chips. The STOPCTLD- (Stop Count Load) input to U26 (U32-, U33-, and U34-generated from U13-11) overrides counting and loads the data present on the parallel data lines into the counter. Each counter chip has a maximum count output that is gated by U38. When all of the counters reach maximum count, the output from U38 puts an active low on the data input of a dual D-type flip-flop (U10). U10 then provides the STOPCNT- input for U19-20 on the next clock pulse. RDMISC- (Read Miscellaneous) from U11-8 enables the U25-10 output, which is bit 1 of the Status Register, to read the status of the Stop Counter. The Stop Counter is programmable for 1 to 64K counts and is used to control SYNC history latches and CRC registers.

I/O Module Interface Connector

The I/O Module Interface Block located on the Probe I/O Module Interface PCA, shown in Figure 3-5 of the functional block diagram, contains three parts.

- The connector and related components for the I/O Connector PCA connector.
- The -VDRV Regulator for the I/O Module Pattern Drive.
- The Overcurrent Detection Circuitry for the I/O Module Pattern Drive.

The I/O Connector PCA Connector interfaces data lines D00 through D15, address lines A01 through A12, and control lines between the I/O Module and the mainframe.

The 16 data lines from the I/O Connector PCA to the Probe I/O Module Interface PCA connect to the uP Data Bus with the low eight data bits direction controlled by an Octal Bus Transceiver (U39). The transceiver's data flow direction is controlled by an RDSL (Read Select) signal generated from PS5-, LDS-, and READ-. The upper eight data bits are unused. The address lines and four control lines (R/W- (Read/Write), FGATE (Frequency Gate), ODRESET (Over Drive Reset), and SEL- (Select)) are buffered by line drivers to maintain signal levels for communication with the I/O Modules and the I/O Connector PCA. The STROBE signal is generated for the I/O Modules by gating NDS- (New Data Strobe) with PS5- (Peripheral Select 5). The STROBE signal is sent to the I/O Connector PCA for further processing before reaching the I/O Module. Outputs from the I/O Module include the two interrupts DCE and IOGEN. The sense + and sense - signals are sourced from the +VDRV voltage regulator on the I/O Connector PCA.

I/O MODULE -VDRV VOLTAGE REGULATOR

This regulator provides a -0.85V output with a high short term current sinking ability (greater than 2A) and a long term current sinking capability of 250 mA. Overload detection is also provided. Figure 3-6 presents a simplified schematic of the -VDRV Voltage Regulator.

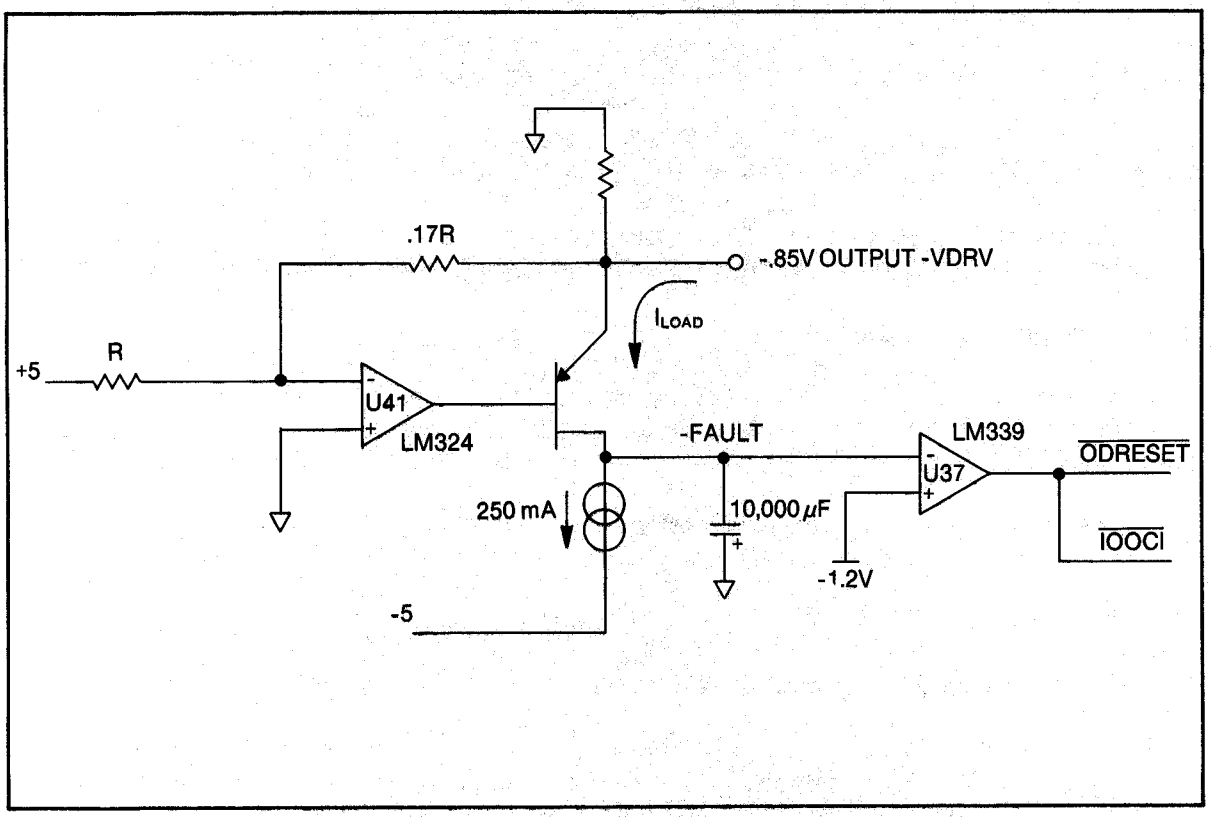


Figure 3-6. -VDRV Voltage Regulator Simplified Schematic

The regulator uses an inverting op amp circuit. With a gain of -0.17, the op amp provides -0.85V output from the 5V input. The PNP power transistor (implemented as PNP/NPN compound Q9/Q10) is configured as an emitter follower and is used to provide increased current sinking capability. The collector supply is a 250 mA constant current sink. Dual Diode CR10 is used to return feedback to U41 and to clamp U41's output during low current situations.

When the current demand is low (less than 250 mA), the current sink saturates, and the -FAULT signal is at about -4.5V. If a high current transient appears, the current sink (Q11 and part of op amp U41) turns on, and 250 mA flows into the -5V supply. The rest of the current flows into the 10,000 uF capacitor, slowly charging it up. Because this capacitor is in the collector circuit of the power transistor, the regulator's output remains unaffected while this voltage is rising. If the current demand is high enough or long enough, the capacitor charges to above -1.2V. At this level, the LM339 comparator trips, generating an

IOOCI- interrupt and forcing the control line ODRESET- low. This in turn shuts off the I/O module overdrivers, limiting the current. The time constants of the circuit are set so that 2A can be sunk for 10 ms without affecting the regulated -VDRV output or generating an overcurrent fault.

I/O MODULE OVERCURRENT DETECTION

I/O Module overcurrent conditions are detected from either of two sources: the +VDRV supply or the -VDRV supply. The +VDRV regulator is situated on the I/O Connector PCB. Current sense from that supply is provided via the sense+ and sense- signals, which are differentially amplified by a section of U41 and compared by a section of comparator U37 to a reference. This reference is switchable, via the LO-CURRENT- line, to one of two settings. The low setting, commanded when LO-CURRENT- is low, sets a reference of about .4V, which in turn sets an effective current limit of about 200mA. The high setting sets the reference to about 4V, which sets the current limit to about 2A. This high current setting is guaranteed by software to never be active for more than 10 ms, (with a max duty cycle of 1%). R73, C18, and CR12 slow down the output of the differential amplifier so that it does not trip on transients.

A -VDRV overcurrent condition is detected by another section of the U37 comparator. These two comparators are "wire ORed" together. If either one detects a fault, both of their outputs goes low. This fault causes the ODRESET- line to go low, which turns off the I/O Module overdrivers, thus removing the overcurrent fault. At the same time, flip-flop U27 is clocked, making IOOCI- go active and generating an interrupt. This interrupt can be cleared by writing line IOCLRINT- low; (WRITE @ C1801: bit 1 = 1 says clear interrupt; bit 1 = 0 says release interrupt).

Miscellaneous Functional Blocks

The Probe I/O Module Interface PCA has two functional blocks for the specific purpose of interfacing with external equipment: the SYNC Pulse Isolation block and the Footswitch Connector (J4). Two other functional blocks (Data Bus Buffers, Status Register, and Control Register) support operations for probe control.

SYNC PULSE ISOLATION

SYNC Pulse Isolation uses an optoisolator and an earth-referenced divider to provide an earth-referenced TTL level SYNC Pulse (isolated from the 9100A/9105A) to an oscilloscope. Inputs to this block include an earth referenced +5 volts and a clock pulse from U2-6. The resulting external trigger output is available at a BNC connector on the rear panel.

FOOTSWITCH CONNECTOR

The Footswitch Connector (J5) is a standard telephone jack that connects to a normally open switch. The switch is used as an external event recognizer. A test program can use such a switch to make a program depend on an external event, a manually generated signal, or a limit. Access to J5 is on the right side of the mainframe labeled (EXT SW). A switch closure is detected by the COLUMN9 and ROW7 signals; these signals are sourced from the keypad scanning circuitry on the Display PCA.

DATA BUS BUFFERS

Data Bus Buffers (U35, U36) permit data transfer from the microprocessor data bus to a buffered data bus. Instructions from the microprocessor to the ICs on the Probe I/O Module Interface PCA move along the microprocessor data bus through J6 to U35 and U36. The data moves through the Data Buffers onto the buffered data bus to the required ICs.

STATUS REGISTER

The Status Register (U25) monitors single data bits on the Buffered Data Bus to detect I/O Overcurrent Interrupts, Probe Power, Stop Counter Status, and Pulse-Transition Counter Carry-Bit Status. The Status Register is a quad 3-state buffer (U25) connected to the output of the circuit and the data bus. U25 is read only, and Figure 3-7 summarizes the status bits. The Status Register output to the data bus is enabled by the RDMISC- (Read Miscellaneous) signal from U11, pin 8.

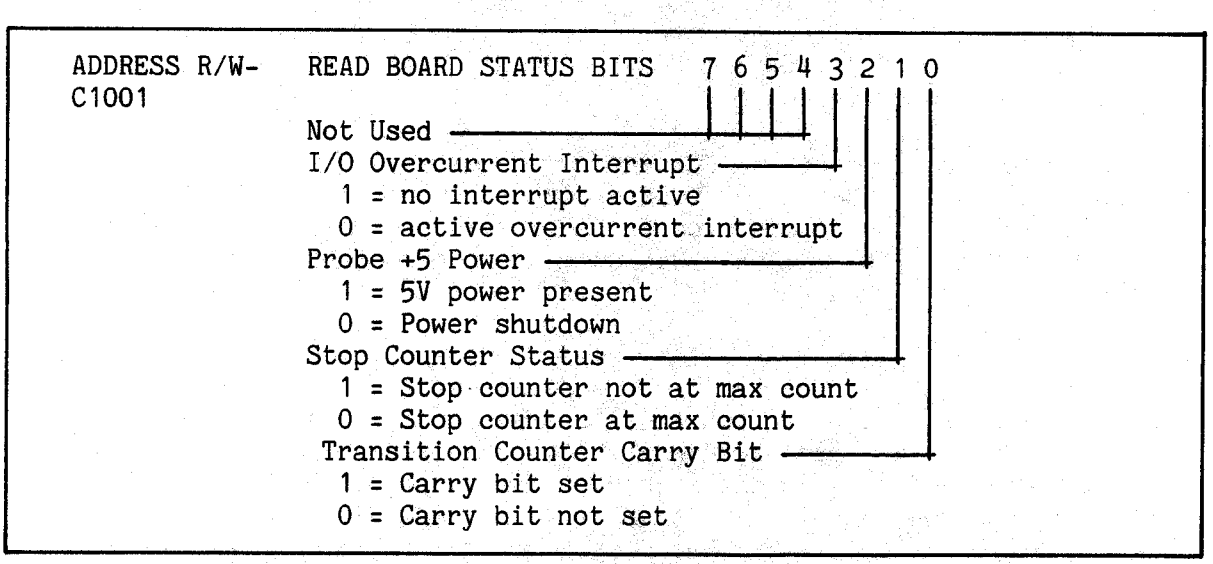


Figure 3-7. Status Register Bit Breakdown

CONTROL REGISTER

A 4-bit Write-Only Control Register (U17) generates the STOPCTENA- (Stop Counter Enable), IOCLRINT- (IO Clear Interrupt), EN0 (Enable 0), and EN1 (Enable 1). The Control Register decodes data bits 00 through 03 of the Buffered Data Bus to generate the output signals. Data bits 02 through 03 determine different ENABLE combinations. Data bit 01 either clears or allows an I/O Overcurrent Interrupt, and data bit 00 enables or disables the Stop Counter. Figure 3-8 represents the data bit breakdown for the Control Register.

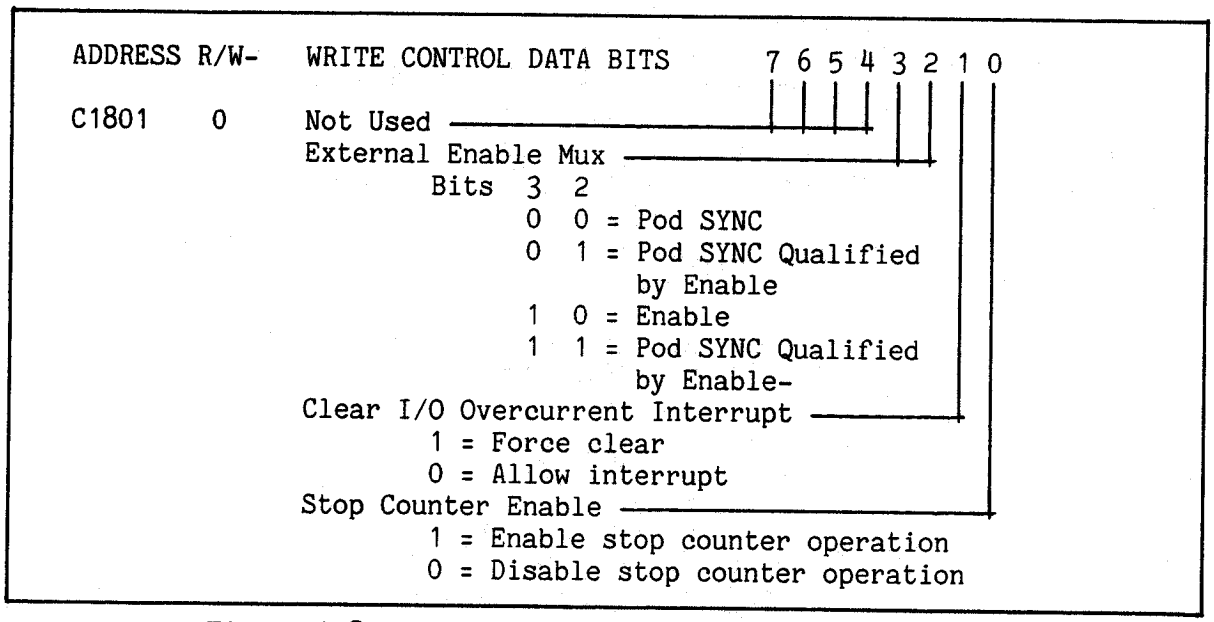


Figure 3-8. Control Register Bit Breakdown

I/O CONNECTOR INTERFACE

Overview

The I/O Module Connector PCA provides the interface for the I/O Module to the 9100A/9105A. The I/O Connector Interface shown in Figures 3-1 and 3-2 is a vertically-mounted PCA that plugs into the Probe I/O Module Interface PCA, which connects to the Main PCA. Up to four I/O Modules can be connected to the 9100A/9105A. The I/O Connector and the Probe I/O Interface PCAs buffer the 68000 microprocessor address and data bus to send data out to the modules. The PCAs also contain the I/O Module overdriver power supplies and circuitry to gather and distribute control, data, and address signals, event detection, and operational power for each I/O Module.

Power Supplies

There are two power supplies for the I/O Module, one at 5V, (called +VDRV), and one at -0.85V (called -VDRV.) The +VDRV power supply is a linear supply derived from the +12V supply. Current is sensed by measuring the voltage across the .47 ohm resistor. This voltage is measured on the Probe I/O PCA from the SENSE +/- lines.

Gross overcurrent protection is provided by an LM338 voltage regulator (U4). Normal overcurrent protection is provided via an overdriver shutdown line, (ODRESET-). This line instantly turns off the overdrivers, removing the overcurrent fault. An overcurrent fault is triggered if current exceeds two programmable levels: 200 mA, and 2A. The 200 mA level is the power-up default, and is only changed to the higher level during pattern drive. The 2A level is a short term (10 ms 1% duty cycle) maximum amount of current for all four I/O Modules. The overcurrent level is controlled by the (LO CURRENT) control line produced by DTIO #2 (U7) on the Main PCA. If the 200 mA and 2A thresholds are violated, an I/O Overcurrent Interrupt (IOOCI) is generated. Simultaneously, all of the overdrivers on all of the I/O Modules are shut off.

The 10,000 uF capacitor is part of the -VDRV regulator, which is covered in the Probe I/O Module Interface discussion.

I/O Module Connector PCA Contents

The I/O Connector PCA contains four DB-37 vertically-mounted connectors that are accessible on the rear panel of the mainframe. On the other side of the PCA is a voltage regulator (U4) with supporting capacitors (.01 uF, 1000 uF), and the 10,000 uF capacitor used in the -VDRV regulator. The connector to the Probe I/O PCA (J1) supplies all I/O Module power, event detection, address, data, and control signals to the I/O Module.

The address bus containing A01 through A11 and the data bus containing D00 through D07 distribute address and data lines to each connector with A08 through A11 used to determine the +/- STROBE for the selected I/O Module. When the STROBE signal is divided between each module connector, the signal has PS5 and "hot bits" decoded in the signal. The Pod +/- SYNC signal used for timing with the Probe and I/O Module is also distributed to the four I/O connectors by a quad ECL-TTL translator (U2).

The DCE- and IOGEN- interrupts from each module are input to a dual 4-input NAND gate (U3). The outputs of U3 are connected to J1 and sent to the mainframe for further processing. The MODSEL- line is connected through jumper J8 to IWAIT3-. This forces I/O Module bus communications to occur with three wait states, allowing for reliable bus operation over long cable lengths.

PROBE/PULSER

Overview

The Single-Point Probe/Pulser is a 9100A/9105A interface device used to measure portions of the UUT PCA not accessible to the I/O Module. The Probe/Pulser measures inputs up to 40 MHz and generates stimulus pulses at up to a 50 kHz rate. A 1-bit-wide data channel provides input measurement and output stimulus capabilities. Features available through use of the Probe/Pulser include: 16-bit cyclic redundancy checks (CRC), clocked and asynchronous level history, and frequency measurements. The Probe/Pulser instrument is divided into four functional blocks:

- Sensing Block (Probe)
- Pulsing Block (Pulser)
- Level Indicator Block (Lights)
- Switch Block (Switch)

Refer to Figure 3-9 for the functional block diagram of the Probe/Pulser.

Probe

The Probe measures signals from the UUT, with the Probe tip making a single-point connection on the UUT board. The UUT signal is routed through Probe circuitry and the Probe cable to the 15-pin Probe connector on the right side of the mainframe. The Probe functional block contains both the common ground and the one-bit data channel for the UUT.

PROBE TIP INPUT

Signals enter the Probe Tip, passing through R1 and R2. These two resistors in conjunction with R8 on the Probe I/O PCA form a resistor-divider compensation network to match the impedance of the Probe cable. R9 is a pull-up resistor to pull the Probe to a tri-state condition when no other inputs are connected. The input signals exit the Probe via J1-14 and enter the Probe I/O Module Interface PCA. The speed of the input signals must meet the criteria listed in Figure 3-10 to be captured by the Probe Data Channel.

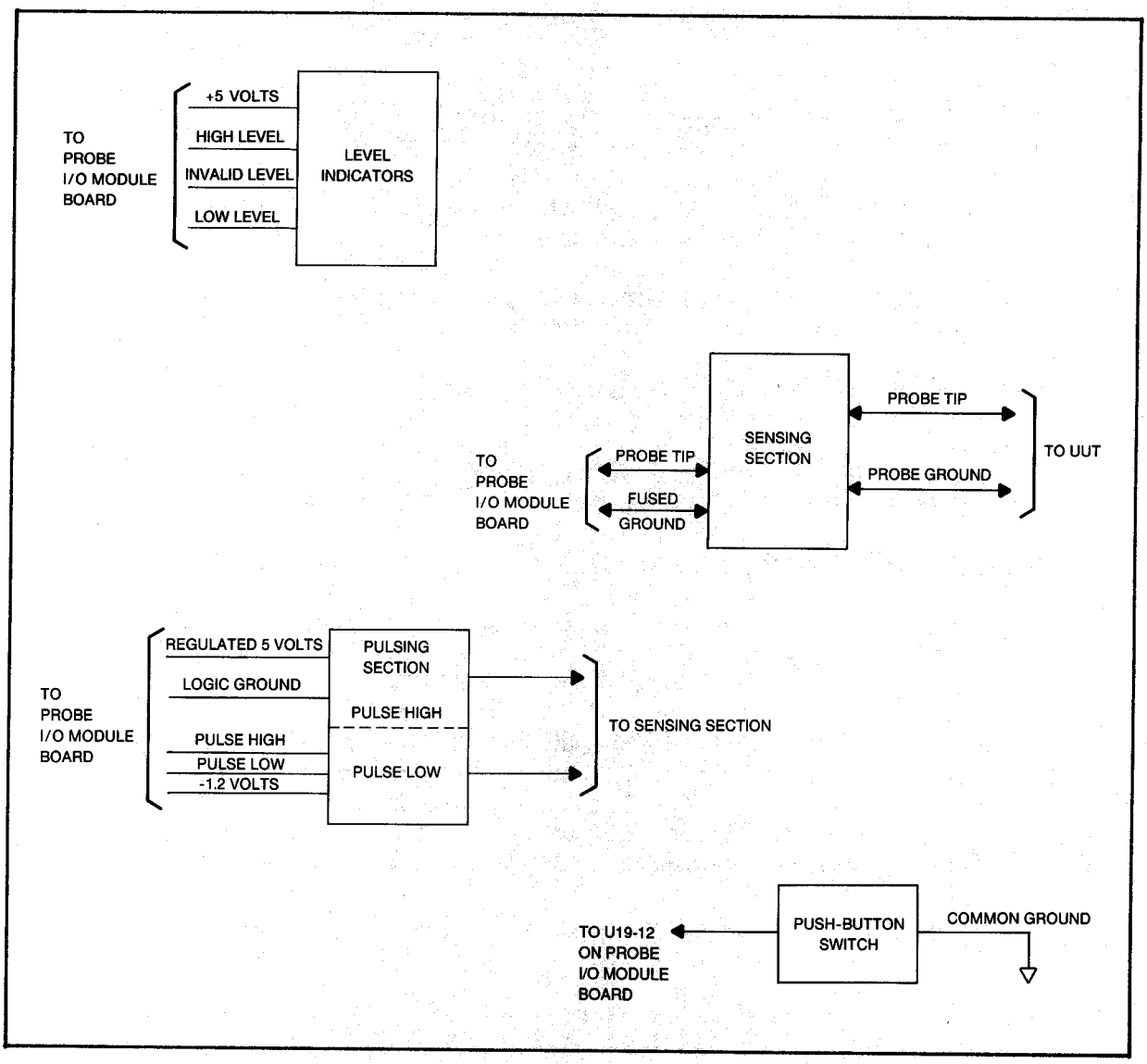


Figure 3-9. Probe/Pulser Functional Block Diagram

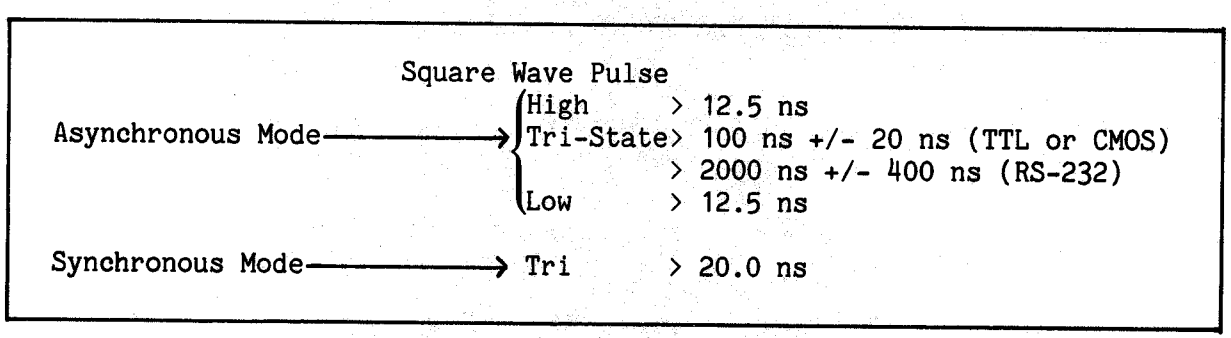


Figure 3-10. Probe Speed Specifications

COMMON GROUND CLIP

The Common Ground Clip connected to the Probe/Pulser clips to the UUT common ground. At the point where the ground connects to the Probe/Pulser, the common lead screws in to make connection. The ground line passes directly through the instrument to J1-9. If the user misconnects the Common Clip, a Probe Fuse located next to the Probe Connector on the mainframe provides protection from power supply shorts or other overcurrent conditions. The Ground Clip must be connected to the UUT to ensure a short return path for pulsing current.

Pulser

The Pulser stimulates input signals for checking output data on the UUT. The Pulser drives a short duration high current level either high or low at a node being tested. The output pulse can be toggled between High and Low or turned off completely (Tristate). During the low pulse, current is supplied by Q4. A high logic level on the PULSE LO signal line turns on Q4, driving the Probe tip low through CR4. C4 supplies instantaneous current for the low pulse. When the Pulse low signal line is off (logic low), Q3 conducts to turn off Q4 quickly. CR4 prevents the Probe tip from being pulled high at this time. The -1.2 input voltage from the Probe I/O Module (J1-13) is used to generate the low pulse.

On the PULSE HI signal line, the logic high into U1-5 inverts to a logic low to turn Q1 on, driving the probe tip high through CR1. C2 is a speed-up capacitor that drives Q1 into saturation, and C3 supplies instantaneous current for the high pulse. A logic low on the PULSE HI line turns Q1 off; Q2 is turned on, and CR1 prevents the Probe tip from being pulled low. The regulated +5-volt supply is used to generate the Pulse High signal and supplies power to U1. Both pulse levels drive the voltage at a specified current for the time shown in Table 3-21.

The Probe pulser exhibits a certain delay in reacting to the synchronous inputs. The maximum propagation timing from synchronous input to pulser action is listed in Figure 3-11.

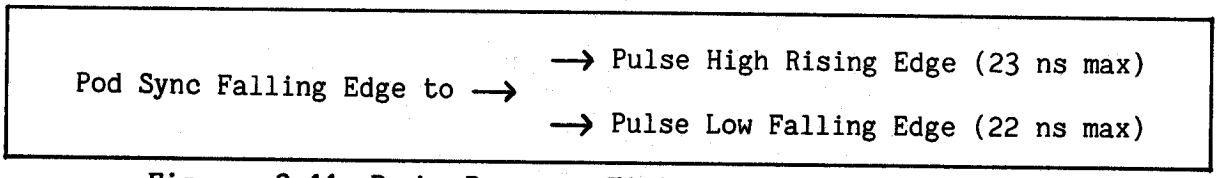


Figure. 3-11. Probe Response Timing Specifications

Table 3-21. Typical Probe Pulser Amplitude

LEVEL	VOLTAGE	CURRENT
High	> 3.5V	200 mA for less than 10 us (1% duty cycle)
	> 4.0V	5 mA continuously
Low	< .8V	200 mA for less than 10 us (1% duty cycle)
	< .4V	5 mA continuously

The minimum pulse widths of the Pulser are shown in Table 3-22.

Table 3-22. Pulser Pulse Width

MODE	WIDTH
Pod Sync	> 50 ns
Free Run	2 us @ 1 kHz pulse rate
External	> 50 ns

Level Indicators

There are three level indicators on the Probe. The level indicators are used to indicate what logic levels have been encountered. The indicators have the following meaning:

- Red: A valid high signal was encountered.
- Yellow: An invalid signal was encountered.
- Green: A valid low signal was encountered.

The logic indicators are driven by a circuit on the Probe I/O PCA that stretches the pulses to a minimum length of 50 milliseconds.

LOGIC LEVEL MODES

The lamp logic can display either in a synchronous or asynchronous logic mode. A writable register in the Probe Custom Logic Chip on the Probe I/O PCA chooses either synchronous or asynchronous mode. The choice is hardware independent of the SYNC Mode of the CRC and other clocked latches. Asynchronous information is displayed when SYNC is set to FREERUN, and all other SYNC modes display the last synchronous data.

LEVEL INDICATOR OPERATION

The three level indicators are driven by three open-collector transistors (Q3, Q4, Q5) on the Probe I/O Module PCA. Three resistors (R11, R12, R13) are connected to the lights to maintain keep alive current flow in the off condition to increase bulb life.

Push Button Switch

A push button located on the Probe allows the user to indicate when the Probe is in place and ready to perform a "read probe". When the user presses the push button, an interrupt is generated by the Probe I/O PCA. The interrupt is shared by the fuse-monitoring circuits and thus requires that a status register in the Probe Custom Logic chip be polled to determine the origin of the interrupt.

CLOCK MODULE

Overview

The Clock Module is an external unit that is plugged into the right side of the mainframe. When used in conjunction with the Probe, the Clock Module samples external events (start, stop, clock, and enable) that are necessary in gathering signatures from the UUT to synchronize data input and output through the Probe.

Clock Module Operation

Four comparators (U1A, U1B, U2A, U2B) are used, with respective start, stop, clock, and enable input thresholds provided by the Probe I/O Module PCA. The inputs go through a divide-by-2 resistor-divider network to the comparators. The other input (0.8V) to the comparator is provided by the Probe I/O Module PCA, giving a threshold of 1.6 volts for external signals. The resulting balanced ECL signals are routed through J6 to the Probe I/O Module Interface. An external ground connection is also provided, with a user-accessible fuse (F1) protecting the circuit in case of inadvertent contact of the ground lead to the power source.

The balanced ECL signals from the Clock Module are converted to TTL level signals on the Probe I/O PCA before being introduced to the Custom Probe Logic chip (U19). A detection circuit is used to sense a blown fuse in the Clock Module. The outputs from the Clock Module are Start, Stop, Clock, and Enable. The Enable signal is multiplexed by the selection multiplexer (U16) signal lines; Pod SYNC, Enable ANDed with Pod SYNC, or inverted Enable ANDed with Pod SYNC produces the EXT ENABLE signal to U19-24.

Clock Module Speed

The clock module timing specifications listed below are valid for all signal lines into the pod.

- Maximum Repetition Rate: 40 MHz square wave
- Minimum Pulse Width: 12.5 ns

MULTI-FUNCTION INTERFACE

Overview

The Multi-Function Interface (MFI) PCA supports peripheral systems for use with the 9100A. A Small Computer System Interface (SCSI) and a Real Time Clock are supported as standard features for the 9100A. A version of this pca (Real Time Clock only) is optional in the 9105A.

Addresses

The MFI Card plugs into J6 (the MFI Card Connector) on the Main PCA. The card is allocated the address space 0B0000 through 0BFFFF. A PAL (U3) on the MFI Card divides the applicable address space among the installed peripheral systems. Line FC2 qualifies these addresses, allowing access only from System Mode.

Clock

The Real Time Clock consists of clock chip U9, 32.768 kHz crystal Y1, and a lithium-battery backup backup circuit centered on B1. A DTACK generator (U10) provides the extended read and write cycles required by the clock. Test point TP3 facilitates monitoring of crystal oscillator Y1. Clock U9 contains internal battery-sustained RAM. The clock is addressed through even bytes at addresses B1000 - B1020.

SCSI

The SCSI (Small Computer System Interface) is structured around a 5380 controller chip (U2 on the MFI PCA). Generally, U2 handles hardware and software interfacing between the 9100A and the SCSI bus. On the 9100A, the bus accommodates a hard disk and hard disk controller accessed through the internal SCSI connector (J2); the hard disk and SCSI circuits are not available with the 9105A. The external SCSI connector (J3) provides SCSI bus connection for additional devices. Controller chip U2 is mapped to the 16 odd addresses B1001 through B101F.

VIDEO

The separate Video Controller PCA supports the Monochrome Monitor or a color monitor. It is supplied with the 9100A Programmer's Station. The Video Controller PCA is available with the 9105A as an option. Note that the video system is character-mapped; in other words, a specific video RAM address maps into a physical location on the monitor screen.

Video Controller

The 9100A Video Controller PCA uses the 2674 Advanced Video Display Controller (AVDC), U1, along with the 2675 Color/Monochrome Attributes Controller (CMAC), U2. The 2674 (AVDC) generates the vertical and horizontal timing signals necessary for the display of data on a CRT monitor. The 2674 is programmed with terminal setup information, providing cursor, blanking, and clock signals to the CMAC. The AVDC is assigned address space 0F0000 through 0FFFFF. In time with horizontal (HSYNC) and vertical (VSYNC) signals, the AVDC addresses Video RAM (U3 and U4) and the Character PROM (U5) on lines DADD00 through DADD11. By using the ASCII codes supplied by the microprocessor (and stored in Video RAM) and the correct display character data stored in the Character PROM, this sequencing yields display characters.

Video RAM

U3 and U4 provide two kilobytes of static video RAM. When addressed over the main address bus (AA01 through AA10), Video RAM is used to store ASCII character codes supplied by the microprocessor over the main data bus (DB00 through DB15). Video RAM uses address space 0E0000 through 0EFFFF.

Video Control sequentially samples these addresses using lines DADD00 through DADD11 and generates display characters using the ASCII codes found at these addresses and the corresponding display character information found in the Character PROM (U5).

Video RAM is shared by both the mainframe processor and the video-generating circuitry. The ASCII codes for display characters are stored in memory at the same addresses used by the Monitor. This memory mapping allows for efficient updating of data on the CRT. Figure 3-12 demonstrates display address mapping.

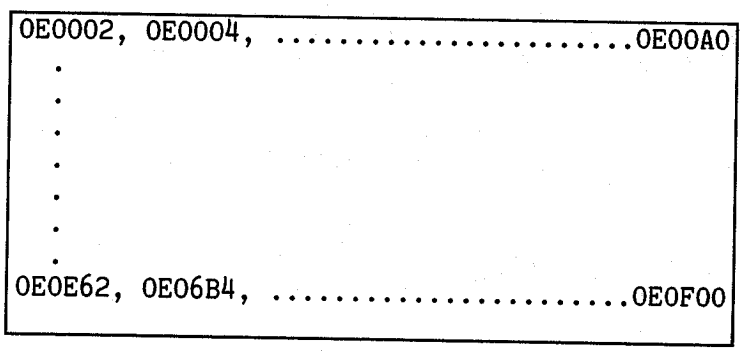


Figure 3-12. Video Display Address Mapping

The video RAM, which resides in a 4K-byte memory space, supplies 2K words for storing characters (1920 words are needed by the 24 lines by 80 characters per line). Both the microprocessor on the Main PCA and the AVDC on the Video Controller have access to video memory; the Main PCA is allowed only to write to video memory. Video control circuitry synchronizes Video and Main PCA requests for memory.

Each displayed character resides in one word of memory, divided into two bytes. Use of the high (or attribute) byte differs between color operation and monochrome operation. The low (or character) byte does not differ between operating modes. Figure 3-13 illustrates the overall data format.

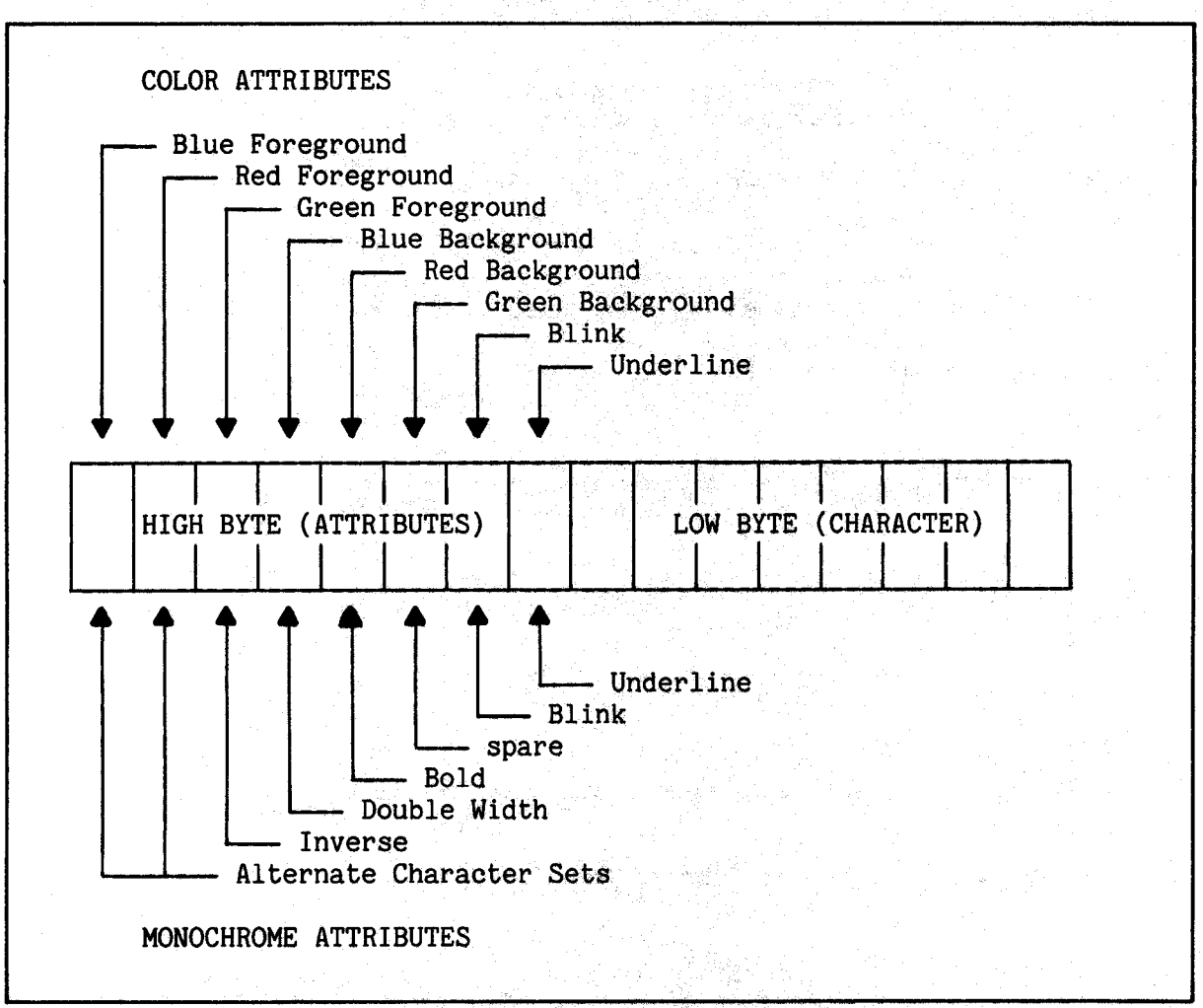


Figure 3-13. Video Character Data Format

The eight registers controlling the video display are selected by the processor using address lines A1, A2, and A3. In addition, line A4 can be high or low for register selection in color mode, but must be high for register selection in monochrome mode.

Outputs to the Monitor include horizontal and vertical sync signals (positive polarity, TTL levels) for both monochrome and color operation. Video data is output as positive white analog levels in monochrome operation or as RGB TTL levels in color operation.

The isolated output allows the mainframe to remain isolated from the earth-grounded monitor. All color and synchronization signals pass through high-speed opto-isolators (U28 - U31). For monochrome output, red and blue output channels are combined to provide high and low intensity signals. Buffer U27 sets the output voltage level, as determined by the red/blue signal intensity encoding. With a color monitor, +5V dc is provided by an earth-grounded power supply on the Main PCA. Otherwise, power from the monochrome monitor is used for enhanced noise immunity.

MONITOR

A separate Monitor can be used with the 9100A Video Controller. A 12-inch monochrome version is available from Fluke. This unit includes a power supply, a CRT, and CRT drive circuitry. Video timing functions are performed by the Video Controller and are not part of the Monitor.

The monitor power supply, which is not manufactured by Fluke, is a switch mode supply that operates from an unregulated 90 to 132V or 180 to 264V ac line voltage and generates the following regulated voltages:

- +12V dc +/- 5%
- -12V dc +/- 10%
- +5.0V dc to +5.1V dc

A color monitor can also be used. See "Color Monitor Specifications" in Section 2 for either the Fluke monochrome monitor or color monitor specifications.

PROGRAMMER'S KEYBOARD

The Programmer's Keyboard is a full ASCII keyboard with additional cursor control and special function keys. Key press codes are sent at 1200 baud in a standard asynchronous format of one start bit, eight data bits (LSB to MSB), and two stop bits. The keyboard buffers up to 31 key codes, at which time the buffer will be filled and subsequent key presses are lost.

The Programmer's Keyboard attaches to the ASCII Keyboard Connector (J10) on the Main PCA. A DUART-Timer-I/O (DTIO#2), U7, provides the Main PCA interface for keyboard signals. The ASCII characters are received as the RxDA input at U7-35.

I/O MODULE

I/O Module Overview

The I/O Module is a device that adds multiple lines of input/output capability to the 9100A/9105A mainframe. The I/O Module has the capability to take CRCs, measure frequency or take event counts, and record logic levels. These measurements can be done simultaneously on up to 40 lines per I/O Module. It is also possible to synchronize the data gathering to the 9100A/9105A uP Pod or to external events using the I/O Module external clock, enable, start, and stop lines. In addition, the I/O Module has the ability to "overdrive" dynamic patterns or static levels onto any of its lines for use in testing devices that cannot be stimulated by the uP Pod. The I/O Module is capable of reading or writing a 40-bit word, and it provides breakpoint capability by generating an interrupt when the data on the inputs equals a programmed value. Input thresholds for each module are selectable between "TTL" and "CMOS" levels. Up to four I/O Modules may be connected to the 9100A/9105A mainframe. The I/O Module consists of seven functional blocks. See Figure 3-14 for a functional block diagram of the I/O Module.

Each of these blocks is described in more detail in the paragraphs that follow:

- Bus Interface Functional Block
- Custom Chip Functional Block
- Clock and Enable Mux Functional Block
- General Control Latch Functional Block
- Connector Code Functional Block
- Input Protection/FET Output Block
- I/O Module Top PCA Functional Block

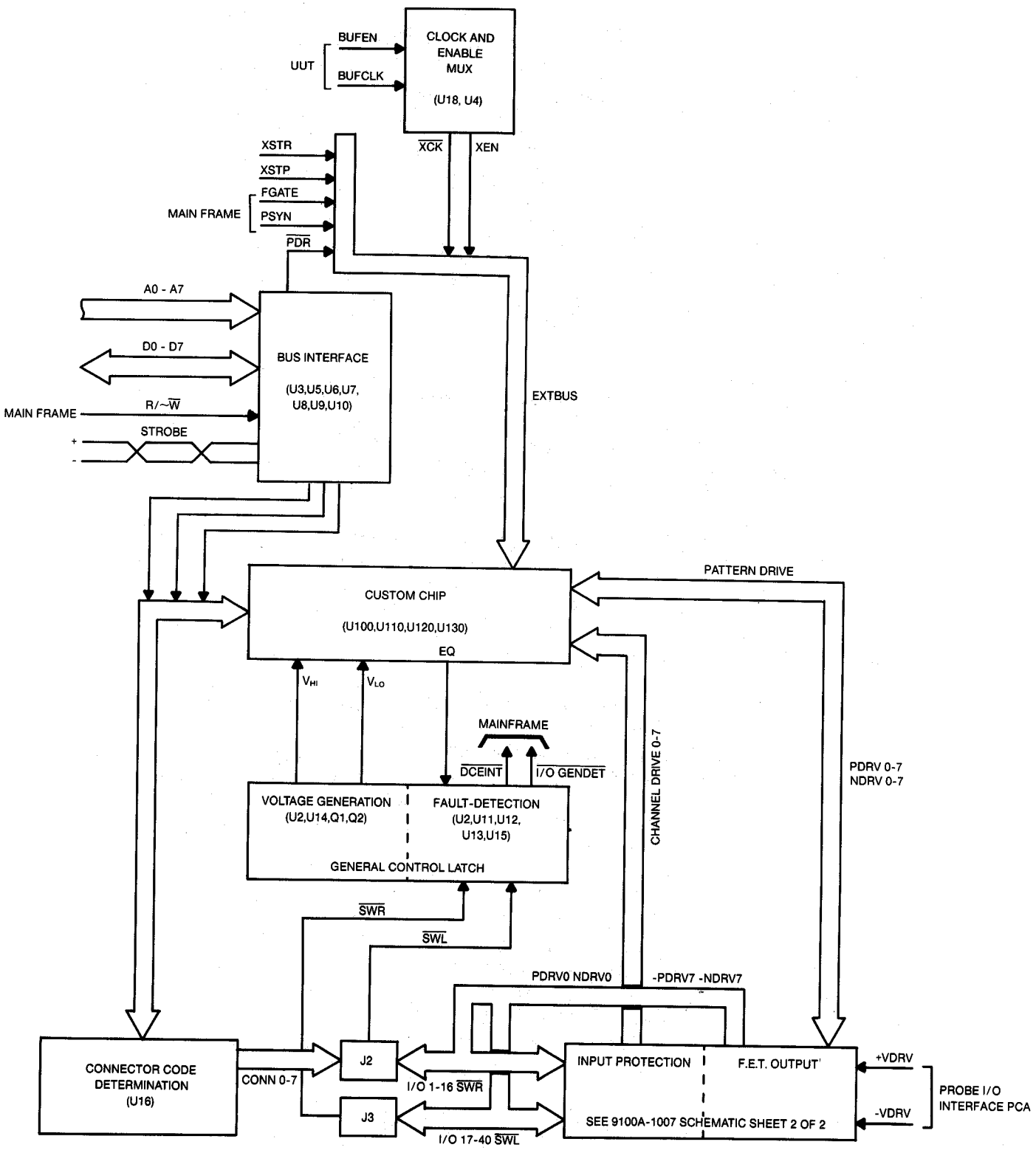


Figure 3-14. I/O Module Functional Block Diagram

Bus Interface Functional Block

OVERVIEW

The bus interface block connects the 9100A/9105A microprocessor bus to the I/O Module. The I/O Module is a memory-mapped device, with all control performed by writes to the I/O Module memory space. A control bus enters the I/O Module on connector J1 and consists of the following lines:

- Seven address lines: A01 through A07
- Eight data lines: D00 through D07
- Two differential strobe lines: STROBE+, STROBE-
- One control line: R/W-

The two strobe signals, which are sent up the cable on a twisted-pair as differential ECL signals, are the key to the clean bus interface. They are translated by U9 into the STROBE- signal. As sent by the mainframe, the STROBE- signal already has some amount of address decoding done in it; STROBE- for any particular module will only be active on accesses to addresses DXXXX, with A0 = 1, and with the proper "hot bit" identifying the module. (See the paragraphs on addresses for more information on hot-bit decoding). STROBE- is the key signal used to qualify all of the bus activities and is used by U7 to latch the addresses and R/W- and to enable the data bus buffer. The STROBE- signal, in conjunction with the latched version of R/W- generates the read strobe (RD-) and the write strobe (WR-). The STROBE- signal and the decoder U6 generate the chip select signals: CS0 through CS4, ADD-, and ADE-.

The following paragraphs explain how the I/O Module address is broken down and what the hex digits signify. I/O Module selection is described with a figure showing which I/O Module(s) are selected. A timing diagram shows typical waveforms during a read and write cycle. The process of enabling the I/O Module custom chip(s) is also described.

ADDRESSING

Memory reserved for I/O Module control occupies addresses D0000 through DFFFF. Out of this 64K-byte block, four I/O Modules can be addressed. Lower Data Strobe, (LDS-), is used to qualify all I/O Module addresses; thus A00 is effectively a 1. Addresses within this space using Upper Data Strobe (UDS-) are unused. Figure 3-15 shows a summary of I/O Module address decoding. Figure 3-16 provides an addressing example.

ADDRESS DECODING

64K block of memory allocated for I/O Modules (D0000-DFFFF)

D 0 X X X

Address lines to all custom chips

MODULE SELECT
Value of Hex digit is a bit mask determining the combination of modules present

ADDR	READ	WRITE
8 9 A B C	Read from chips	Write to chips
D	Read intrpt reg	Write control
E	Read connect code	--not decoded--
F	All chips - alias	Write all chips

Hex value determines the custom chip enabled

Output from U6

The bits of the interrupt register are read to monitor interrupt and general I/O Module status. The bits are:

BIT	DESCRIPTION
7	Threshold status
6	Clk mux status
5	Enable mux status
4	Ground (0)
3	Fuse blown
2	Push button (right)
1	Push button (left)
0	DCE (Data Compare Equal)

The bits of the control register are written to reset interrupts or to perform general control functions. The bits are:

BIT	DESCRIPTION
7	Threshold (1=TTL)
6	Clk mux (0=XCLK)
5	Enable mux (0=EXTENA)
4	--not used--
3	Clr fuse blown (0=clr)
2	--not used--
1	Clr gen intrpt (0=clr)
0	Clr DCE intrpt (0=clr)

Bits 5 and 6 in the control register select the signal that appears on the XEN and XCLK lines, as follows:

CLKMUX	ENAMUX	XEN	XCLK
0	0	BUFENA	BUFCLK
0	1	PSYN	BUFCLK
1	0	BUFENA	CALCLK1
1	1	PSYN	CALCLK2

Figure 3-15. I/O Module Address Decoding Summary

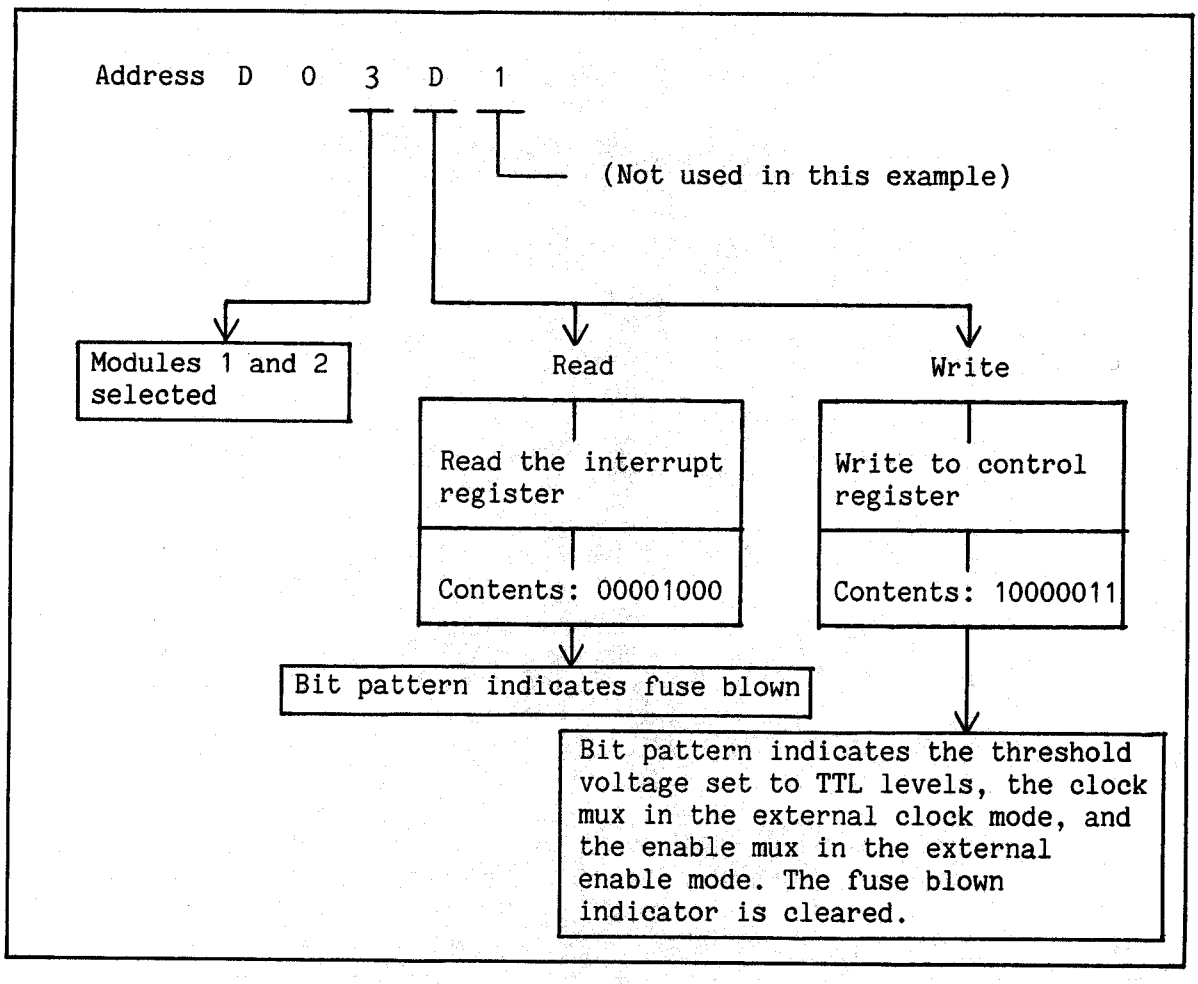


Figure 3-16. Address Decoding Example

Each of the four I/O Modules is controlled via "hot-bit decoding" of address lines A8 through A11. This method of decoding allows any combination of modules to be addressed simultaneously. A brief explanation of "hot-bit decoding" requires examination of the 5-digit hex I/O Module address. The third LSD of the address is broken down into binary form. The position of the set bit(s) determines the module(s) to be addressed. See Figure 3-17 for examples.

The timing diagram, Figure 3-18, shows the signals contained in the bus interface block during a read and write cycle. Each transition point is further explained.

- o A: Address appears on bus, and R/W- goes high signifying a read cycle.
- o B: RD- and CS- go active. Data bus transceiver U8 turns on, pointing toward the mainframe. Addresses and R/W- are latched by U7 and are guaranteed valid.
- o C: Valid read data appears on data bus.

Address	D 0 1 X X	I/O Module 1
	D 0 2 X X	I/O Module 2
	D 0 4 X X	I/O Module 3
	D 0 8 X X	I/O Module 4
	D 0 9 X X	I/O Modules 1, 4
	D 0 F X X	I/O Modules 1, 2, 3, 4
Binary Breakdown	0 0 0 1	I/O Module 1
	0 0 1 0	I/O Module 2
	0 1 0 0	I/O Module 3
	1 0 0 0	I/O Module 4
	1 0 0 1	I/O Modules 1, 4
	1 1 1 1	I/O Modules 1, 2, 3, 4

Figure 3-17. Hot-Bit Decoding Examples

- D: STROBE-, RD-, and CS- return high. Read data guaranteed valid here.
- E: End of read cycle.
- F: Address appears on bus and R/W- goes low signifying a write cycle.
- G: WR- and CS- go active. Data bus transceiver U8 turns on, pointing toward the I/O Module. Addresses and R/W- are guaranteed valid.
- H: STROBE-, WR-, and CS- return high. Write data latched into I/O Module registers.
- I: End of write cycle.

CUSTOM CHIP SELECTION

One use of the Bus Interface is to decode address lines A01 through A07 from the mainframe to determine which custom chips are enabled. As the address signals enter the Main I/O Module PCA through J1, the address lines are latched by U7 (the latch signal is STROBE-). Address lines A07 through A04 are used as address inputs for the decoder (U6). The outputs of U6 are gated to determine which custom chip is enabled. Any one of the five custom chips, or all five may be addressed simultaneously. Particular combinations of the custom chips are not addressed within a module.

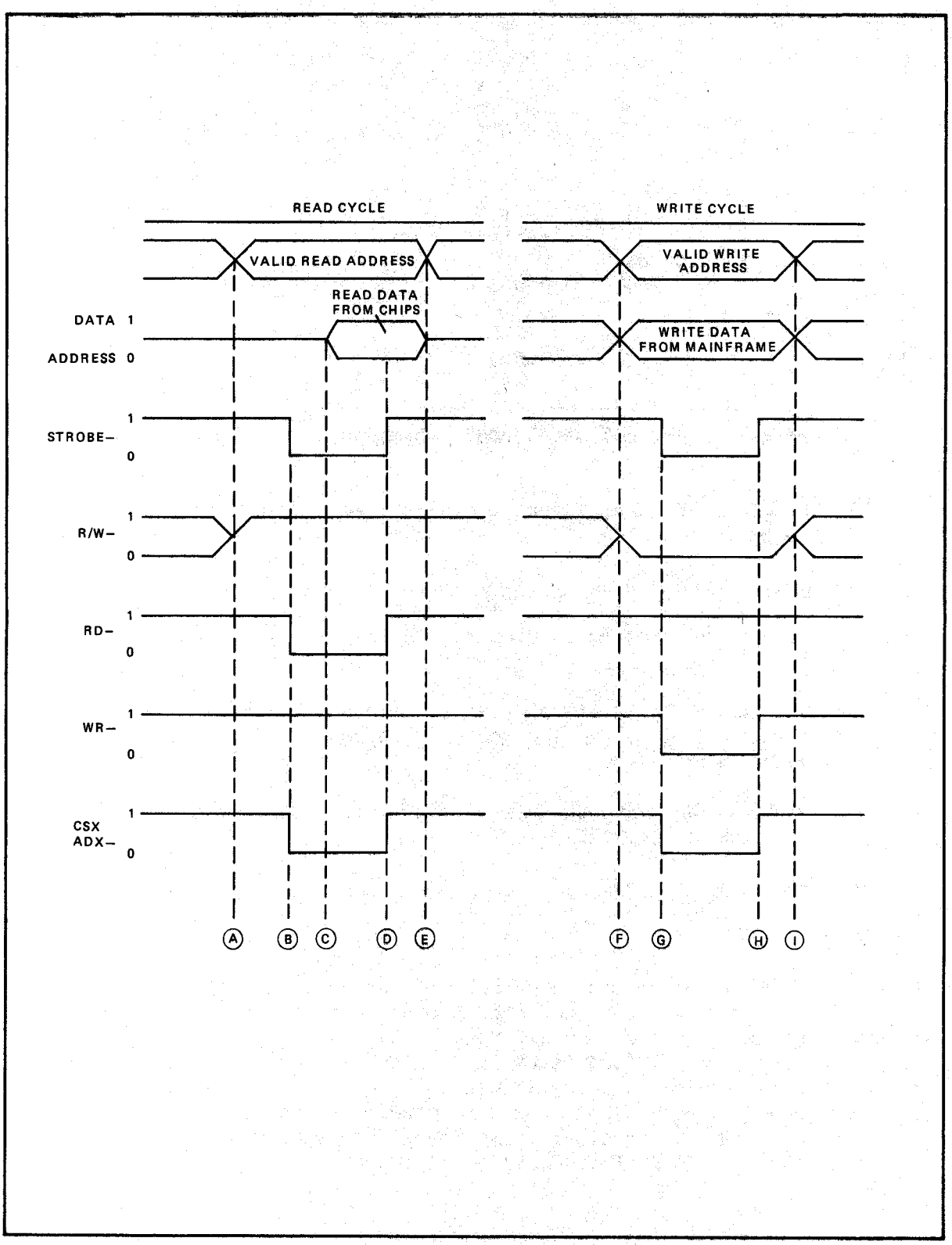


Figure 3-18. Bus Interface Timing Diagram

For example, to select "custom chip U100", the input at U7-13 (A07) from the address bus of the mainframe is at logic low, and U7-18 (A04), U7-17 (A05), and U7-14 (A06) are at logic high. At the occurrence of a strobe signal, U7 latches the logic levels on these pins. At the output signals of U7, LAT-A7 is logic high, and LAT-A4, LAT-A5, and LAT-A6 are logic low. U6 decodes the latched address lines and sets output line AD8- low. The logic low on AD8- is gated and sets up a logic low on CS0-, thereby enabling "custom chip U100". If this were to occur on I/O Module 3, address D0481 would be written.

A custom chip may be addressed individually, or all custom chips may be addressed simultaneously. Address bits A04 through A07 are used to determine custom chip selection. To address all chips, an address in the form DXXFX must be used. This address causes the ALLCHIP signal (U6-7) to go active, making all five chip selects active.

Custom Chip Functional Block

The custom chips each contain eight channels of data acquisition. Each channel performs 16-bit Cyclic Redundancy Checking (CRC), 23-bit (with overflow) transition counting, 3 bits of asynchronous level history recording, 3 bits of synchronous level history recording, and 1 bit of data comparison. The custom chips are used for I/O Module control, and they connect to the data bus via U8. Eleven internal registers control the custom chip. These registers are controlled by Address lines A01 through A03, and the R/W- line.

The pin-out of the custom chip is shown in Table 3-23.

Clock and Enable Mux Functional Block

The Clock and Enable Mux block is located on the I/O Module Main PCA and is shown in the I/O Module Functional Block Diagram, Figure 3-14. Two ICs make up this block: the 74HCT153 (U18) Dual 4:1 Select Multiplexer and the 74HCT04 (U4) Hex Inverter. This block selects one of three sources for the XCK- signal, and one of two sources for the XEN signal.

CLOCK AND ENABLE MUX OPERATION

Inputs

The Clock and Enable block receives inputs from the BUFENA (Buffer Enable) and the BUFCLK (Buffer Clock) signal lines. These signal lines originate from the XCLK (External Clock) and XENA (External Enable) lines. The PSYN (Pod Sync) signal obtained from the EXT-BUS (External Bus) is an alternative clock signal to the external clock and is used for data gathering by the custom chip(s). U18 inputs: POD SYNC, CALCLK1 (Calibration Clock 1), and CALCLK2 (Calibration Clock2) are all clock signals used by the Clock and Enable Mux Block. The POD SYNC signal, which enters the I/O Module as differential ECL, is converted by U9 into TTL levels. This signal enters the EXT-BUS to be used in conjunction with CALCLK1, CALCLK2, ENMUX, and CLKMUX.

Table 3-23. Custom Chip Pin Description

PIN	TYPE	FUNCTION
A0-A2	Input	Address lines
POR-	Input	Power-on reset
SRCK	Input	1 MHz Serial-to-Parallel conversion clock
PDRV0-PDRV7	Output	Pattern Drive PMOS gate drive
NDRV0-NDRV7	Output	Pattern Drive NMOS gate drive
VDD1	Input	Positive voltage supply
VDD2	Input	Positive voltage supply
GND1	Input	Logic common
GND2	Input	Logic common
XD0-XD7	Input/Output	Microprocessor data bus
EQ	Output	Equal (data comparison match) output
TC	Output	Test clock output
WR-	Input	Write enable
RD-	Input	Read enable
CS-	Input	Chip select
VPAT	Input	Negative supply for DRV outputs
TEN	Input	Test mode enable
XSTP	Input	External stop
GATE	Input	Frequency gate input
XSTR	Input	External start
XEN	Input	External enable
XCK	Input	External clock
PSYN	Input	Pod sync clock
VLO	Input	Low voltage threshold select for CD0-CD7
VHI	Input	Hi voltage threshold select for CD0-CD7
CD0-CD7	Input *	Channel inputs
TLI	Input	Test channel comparator input
TLO	Output	Test channel comparator output

* CDn inputs have an internal resistor network to control the voltage at which they will float (the "invalid" voltage). This voltage is approximately 1.6V, through an effective resistance of >50 kilohms.

The CALCLK2 signal enters the Main I/O PCA through the Connector Code Determination Block. CALCLK 1 is not used. Channels 1 through 39 are tied together and to CALCLK 2 when the Calibration Module is plugged in. CALCLK2 is an input to U18-13. The ENMUX and CLKMUX signals are generated by the Control Register (U14-15 and U14-16, respectively) and are control inputs to U18. U18 generates outputs XEN and XCK. Table 3-24 shows which signals appear on the outputs of the multiplexer for all four states of the control inputs.

Table 3-24. U18 Truth Table

Control In		Outputs	
CLKMUX	ENAMUX	XEN	XCK
0	0	BUFENA	BUFCLK
0	1	PSYN	BUFCLK
1	0	BUFENA	CALCLK 1
1	1	PSYN	CALCLK 2

Outputs

The Clock and Enable MUX block outputs XEN and XCK- signals to the EXT-BUS. These two control signals are sent to each custom chip. Three parallel inverters invert the XCK signal from U18-9, and are necessary to ensure a fast rise time into the relatively high capacitance XCK- line.

General Control Latch Functional Block

OVERVIEW

The General Control Latch block, located on the I/O Module Main PCA, is used to vary input thresholds, clear fault conditions, and control the Clock and Enable Multiplexer. Refer to Figure 3-14 for the block's functional relationship on the block diagram. The ICs in this block include: a 74LS273 (U14) 8-bit latch, an LM324 (U2) quad op-amp, two 2N3906 (Q1, Q2) PNP transistors, a 74LS08 (U3) quad 2-input AND gate, a 74LS30 (U15) 8-input NAND gate, and two 74LS112 (U11, U12) dual JK negative-edge-triggered flip-flops.

CONTROL REGISTER

Data lines from the A-D-BUS to U14 produce DCECLR- (Data Compare Equal Clear), GENCLR- (General Clear), FUSCLR- (Fuse Clear), ENMUX (Enable Multiplex), CLKMUX (Clock Multiplex), and THRSH (Threshold) signals. U14 is accessed by a write to DXXDX, where the ADD- and WR- latch data into U14. The Control Register (U14) is cleared by a PWRUP (Power Up) signal held low by C44 to ensure a proper reset.

The J2 and J3 connectors provide the input to the General Control Latch block for detection of Clip and Calibration Modules. J2-25 and J3-6 are the input pins to a detection circuit that provides the SWRDET (the right-hand or B Switch Detect) and SWLDET (the left-hand or A Switch Detect) signals to generate an interrupt. The mainframe reads the interrupt register to determine the reason for an interrupt.

DATA COMPARISON INPUTS

All 40 lines of the I/O Module are compared to a programmable 40-bit data register and qualified by a programmable 40-bit "don't care" register. This comparison is done inside the custom chip(s), eight lines per chip. The EQ outputs (pin 55 of the custom chip), are gated together, and, when they are all high (i.e., a comparison has been detected), an interrupt is generated.

FUSE DETECTION

The FUSEDET (Fuse Detect) is a part of the Multi-Detection area, General Control Latch Block. A 1A slow-blow ground fuse located on the I/O Module Main PCA is used to protect the ground line. The FUSEDET signal becomes an input to the interrupt register (U13-8), along with the other detection signals.

DATA COMPARISON and GENERAL INTERRUPTS

The General Control Latch block outputs detection and interrupt signals for any problems or special operations of the I/O Module. Also, an external DCE pin allows the user to examine the state of the I/O Module hardware.

The following two interrupts are produced by the General Control Latch block:

- DCEINT- (Data Compare Equal Interrupt)
- IOGENINT- (I/O General Interrupt)

The Data Compare Equal Interrupt

The DCEINT- is generated by the I/O Module when the programmed data compare register matches the input data. The DCEINT- signal originates from the EQ pin of each custom chip. The EQ signals are gated to form a DCE- signal. The DCE- signal triggers a J-K flip-flop to produce the DCEDET and DCEINT- signals.

The I/O General Interrupt

The IOGENINT- is an interrupt generated by the I/O Module when either pushbutton on a clip module is pressed. The interrupt status register on the I/O Module must be read to determine the cause. In the case of a button push, two J-K flip-flops output the SWLDET (A side) and SWRDET (B side) signals. These signals are gated to produce the IOGENINT- signal.

Data Compare Equal Output Pin

DCE output pin P1-6 can be used to trigger a logic analyzer or oscilloscope. Buffers and protection circuitry safeguard the DCE signal output.

OPERATION OF GENERAL CONTROL LATCH BLOCK

The General Control Latch Block is divided into three areas. These areas produce voltages for I/O Module operation and contain circuitry that generates detection for a blown fuse. The functional block contains the following areas:

- o Threshold Voltage Generation
- o Multi-Detection and Interrupt
- o Fuse Blown Detection

Threshold Voltage Generation

Threshold Voltage Generation produces the threshold voltages necessary for control of data input to the custom chips. Data Bit 7 of the command register (U14) determines the level of threshold, with a 1 selecting TTL, and a 0 for CMOS. See Figure 3-19 for the command register bit positions.

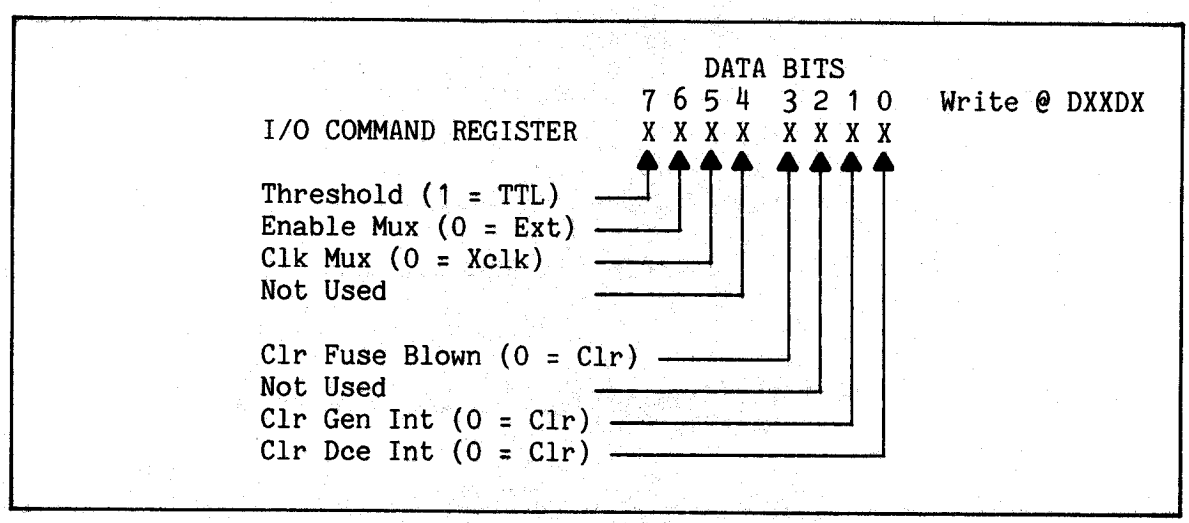


Figure 3-19. I/O Module Command Register

The threshold (THRSH) signal output of U14-19 passes through circuitry that produces a low voltage level (VLO), and a high voltage level (VHI). These voltage levels are used by the custom chips pins 39 and 45 to define the logic low, invalid, and logic high voltage ranges. A logic high out U14-19 designates a TTL logic level and a logic low for CMOS. The THRSH signal controls resistor dividers that are used to create the VHI and VHO signals. Two parts of op amp U2 and transistors Q1 and Q2 are used together to provide a regulated output with high current sinking capability. Typical current seen by these regulators can vary from 10 to 40 mA. Approximate VHI and VLO levels generated are listed in Table 3-25.

Table 3-25. VHI and VLO for TTL and CMOS Logic Levels

DESC	THRSH	VHI	VLO
TTL	1	-1.0V	-2.4V
CMOS	0	-0.25V	-2.2V

Within the custom chip, a voltage level-detection system uses data inputs, VHI, and VLO voltage levels to detect a high voltage input, a low voltage input, or a tristate situation. See Figure 3-20 for an illustration of detection circuitry within the custom chip.

NOTE

The actual input thresholds for the high and low comparators are computed from the formulas shown in Figure 3-20.

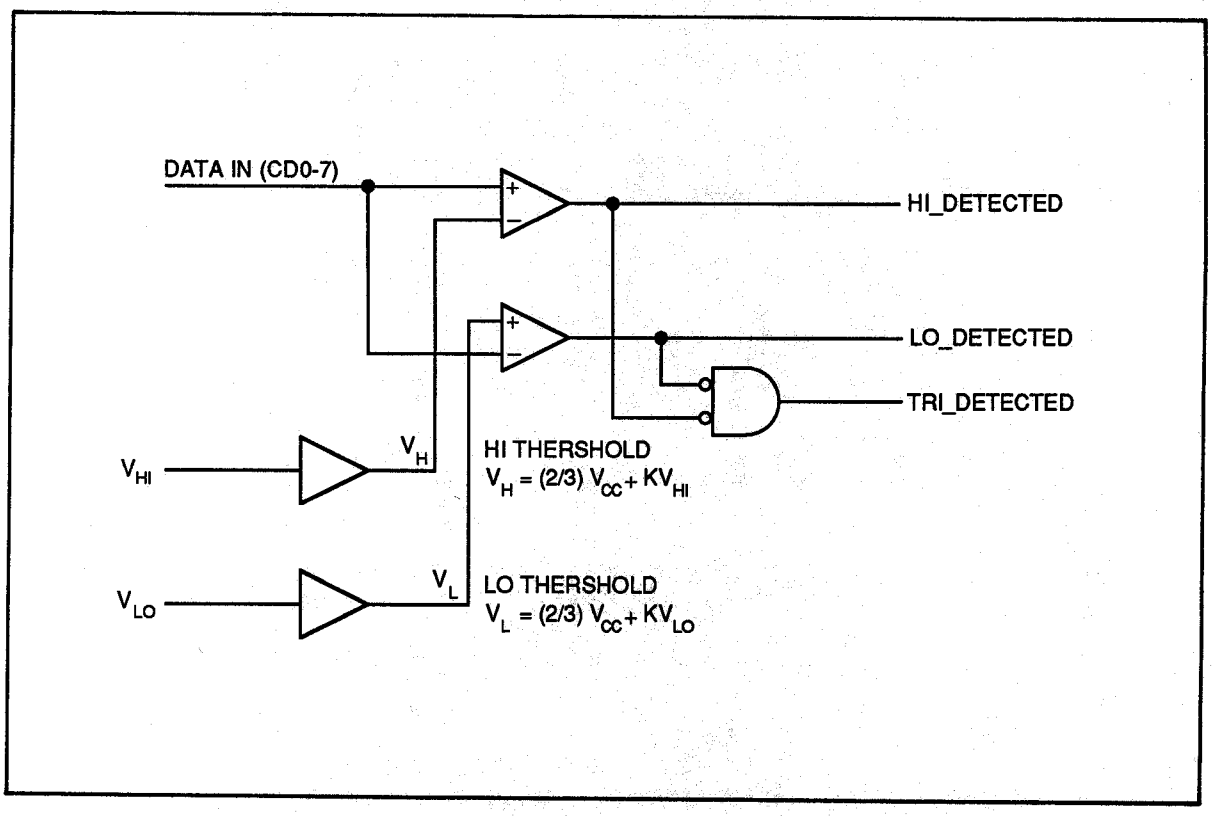


Figure 3-20. Custom Chip Voltage Level Detection

Multi-Detection and Interrupt

The I/O Module accepts different sizes of clip modules. A detection system within the I/O Module is necessary for the mainframe to know the size of the clip that has been installed on the I/O Module. Clip Modules are available in a half-size module and a full-size module. The half-size module plugs into one connector (either J2 or J3), and the full-size module plugs into both connectors (both J2 and J3). Together, clips plugged into both J2 and J3 generate an 8-bit code that can be decoded by the mainframe identify the plugged-in clips.

Fuse Blown Detection

Detection of blown fuses is performed by two LM324 (U2) op-amps and one part of U3 configured as a window detector. If the XGND signal exceeds a +/- 100 millivolt window, U3-6 will go low, forcing the FUSEDET line to go high. This means that when the Interrupt Register is read (READ @ DXXDX), a 1 in bit 3 indicates the fuse is blown. This blown fuse indication is cleared by writing to the I/O Command Register (WRITE @ DXXDX) with a data value having bit 3 = 0.

Connector Code Functional Block

The components associated with the Connector Code block are the 74HCT244 (U16) Octal buffer/line driver and part of J2 and J3 connectors. This block is located on the I/O Module Main PCA as indicated on function block diagram Figure 3-14.

The mainframe determines which Clip Module the user has installed by reading and decoding connector codes embedded in each Clip Module. To read the code, the mainframe performs a read @ DXXE1. This operation generates the ADE- signal, which in turn enables U16, placing the code on the data bus. Of the eight bits read, the lower four bits refer to the "A side", and the upper four bits refer to the "B side". Thus, differentiation is possible for 16 different conditions on each side of the module. Clips that use up an entire module use an 8-bit code. The most significant nibble of these codes is 1110. For a list of the codes, see Table 3-26.

Table 3-26. Dip-Clip and Calibration Module Configuration Codes

4 BIT CODE	MEANING
0000	14-Pin Clip
0001	16-Pin Clip
0010	18-Pin Clip
0011	20-Pin Clip
0100	24-Pin Clip
0101	(reserved)
0110	Used as most significant byte of calibration header
0111	(reserved)
1000	(reserved)
1001	(reserved)
1010	(reserved)
1100	(reserved)
1101	20-Pin Flying Lead Set
1110	Full width connector, use other 4 bits for ID
1111	No Clip Installed

8 BIT CODE 7654 3210		MEANING
1110	0000	28-Pin Clip
1110	0001	40-Pin Clip
1110	0010	Calibration Header
0110	0010	Calibration Header
1110	0011	(reserved)
1110	0100	(reserved)
1110	0101	(reserved)
1110	0110	(reserved)
1110	0111	(reserved)
1110	1000	(reserved)
1110	1001	(reserved)
1110	1010	(reserved)
1110	1011	(reserved)
1110	1100	(reserved)
1110	1101	(reserved)
1110	1111	(reserved)
1111	1111	No Clips Installed

CONNECTOR CODE EXAMPLES

If the connector codes are to be determined on I/O Module 3, a Read @ D04E1 would be performed. Table 3-27 presents some examples of codes and their interpretation.

Table 3-27. Connector Codes

DATA READ	MEANING
F3	No clip on B side, 20 pin clip on A side
4F	24 pin clip on B side, no clip on A side
E1	40 pin clip installed
14	16 pin clip on B side, 24 pin clip on A side
FF	no clips installed

Input Protection/FET Output Block

OVERVIEW

The Input Protection/FET Output Block combines the functions of input channel protection for each custom chip and output for the I/O Module. Input protection clamps overvoltage, undervoltage, and static conditions before they reach the custom chip.

The output circuitry uses complementary N and P channel DMOS FETs. These FETs can be commanded to drive the I/O line high or low or leave it undriven (off). The custom chip drives these FETs through a 74HC244 buffer. Figure 3-21 shows a simplified circuit of a single channel. All 40 channels are functionally identical to each other.

This output circuit uses power supplies +VDRV and -VDRV. These voltages are generated, regulated, and current limited on the Probe I/O and I/O Connector PCAs. The nominal voltages for these supplies are 5 volts and -0.85 volt, respectively.

INPUT PROTECTION SECTION OPERATION

Data from the I/O lines travels through its respective connector into the protection circuit. Diodes connected to +5 volts and ground protect the custom chip from undervoltage and overvoltage.

FET OUTPUT SECTION OPERATION

The output block can assume three states: high, low, and off. The output block, in conjunction with the input block, allows for measurement of signals at the inputs. The truth table shown in Table 3-28 lists the logic levels of NDRV and PDRV.

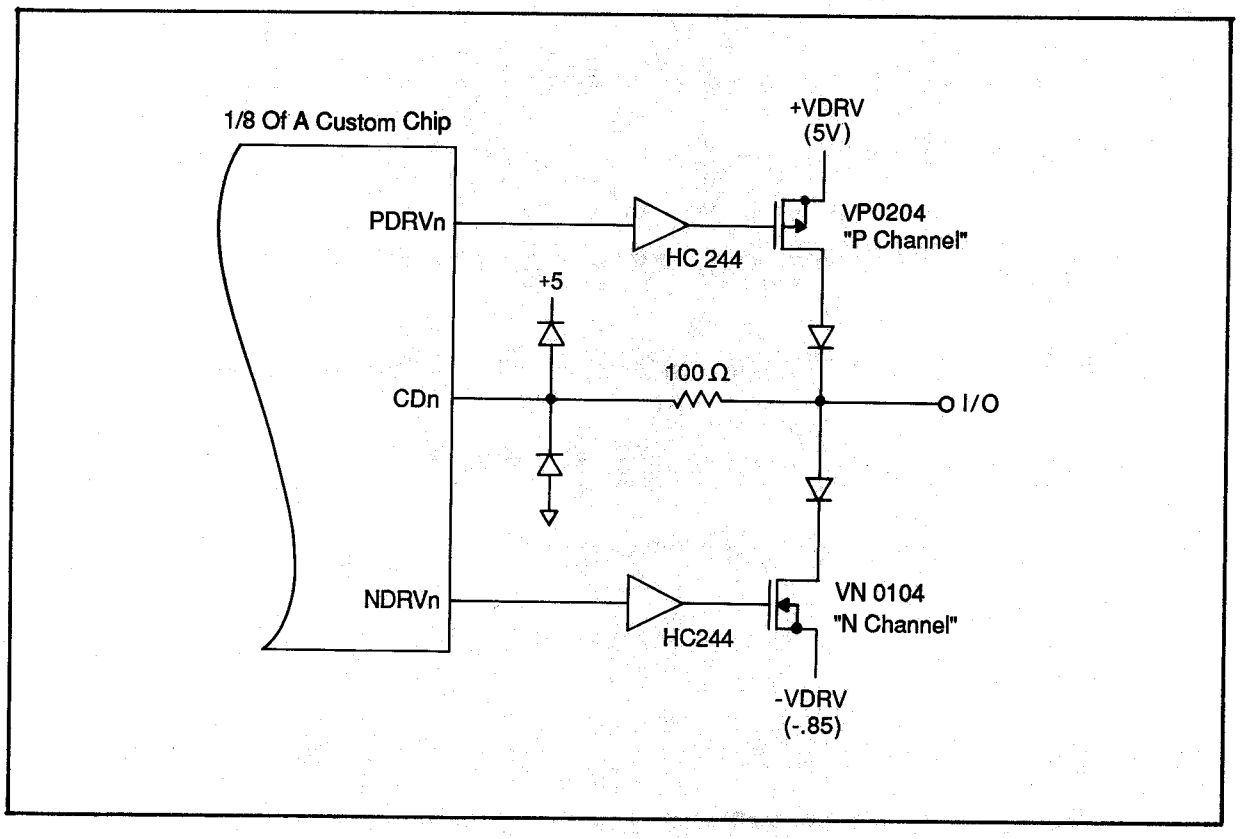


Figure 3-21. Chip Channel Input/Pattern Drive Output Simplified Schematic

Table 3-28. Logic Levels of NDRV and PDRV

OUTPUT	NDRV	PDRV
HI	0	0
LO	1	1
OFF	0	1
(illegal)	1	0

I/O Module Top PCA Functional Block

The top PCA of the I/O Module is a four-layer board consisting of connectors J2 and J3, banana plugs P1-P4, headers J1 and J4, and four 4700 uF capacitors. The top board connectors (J2, J3) provide the input for the 40 I/O lines from the Clip or Calibration Module. The four capacitors together form an effective 4700-uF bipolar capacitor. This is placed across the ground fuse to lower the fuse impedance. P1-P4 represent reference plug-in points between the plug-in module and the I/O Module for external ground and signal ground. The top I/O Module PCA allows for plug-in of a half or full Clip Module or a Calibration Module. These modules plug into J2 and/or J3 of the top PCA and transfer I/O lines to J2 and J3 of the I/O Module Main PCA. P1 and P3 are the signal ground connection points between the I/O Module and the Clip Module. P2 and P4 are the external ground connection points. These connection points improve grounding by providing multiple paths between the clip modules and the I/O Module.

DIP CLIP AND CALIBRATION MODULE FUNCTIONAL BLOCK

The Clip Module is a 9100A/9105A system accessory that offers the user a selection of configurations to test UUT I/O lines. There are two different sizes, a half width and a full width. The number of pins each size can handle is explained in the following paragraphs. The Calibration Module is another unit that the user installs onto the top of the I/O Module for calibration of clock signals.

Overview of the Clip and Calibration Modules

The Half-Width Clip Module is used for connecting the I/O Module to an IC. Five modules are available, in 14-, 16-, 18-, 20-, and 24-pin configurations. If one of these IC clip modules cannot be used, a 20-pin flying lead set is available.

The Full-Width Clip Module connects the I/O Module to 28- and 40-pin IC configurations. The Full Width Module contains two connectors to provide access for up to 40 I/O lines and a ribbon cable attached to either a 28- or a 40-pin IC clip.

The Calibration Module helps perform I/O Module calibration by assuring that simultaneous level transitions occur at both the clock and data inputs of the I/O Module. The clock and data inputs are recorded simultaneously by the latches in the I/O Module. The Calibration Module attaches to the two I/O Module connectors (J2, J3).

Clip and Calibration Module Operation

HALF WIDTH CLIP MODULE

The user plugs the Clip Module into the top of the I/O Module, then attaches the clip connected to a ribbon cable to the UUT. The Half Width Module can be connected to J2 (A side) or J3 (B side) of the I/O Module.

NOTE

Check the schematic for the I/O signals lines used in each case.

An SPST four-position dip switch contained in the Half-Width Module determines the code for the module. This code tells the mainframe the type of pin configuration used during the current I/O test. The connector code is factory set, and should not be changed. For a list of connector codes, see Table 3-27. A black ID button located on the front of the module housing can be used to signal the mainframe.

FULL-WIDTH CLIP MODULE

The Full-Width Module connects to IC chips under test (28- and 40-pin configurations). The Full-Width Module uses the same procedures and tests as the Half-Width Module. The Full-Width Module uses both I/O Module connectors for the additional I/O signal lines.

To identify the connection code of the Full-Width Module, the Module contains an SPST eight-position DIP switch. The Full-Width Module requires an 8-bit connection code so that the mainframe can determine the size of the clip the user has plugged into the I/O Module. A black ID button located on the front of the Full-Width Module is used to signal the mainframe.

CALIBRATION MODULE

The Calibration Module is used in calibrating both the delay between the data input and the external clock output and the delay between the data input and the pod synchronous clock. The Calibration Module ties channels 1 through 39 and CALCLK2 together. Channel 40 is connected to a "Flying Lead" and is used for calibration to the pod. With the Clock Multiplexer (U18) signal properly programmed, CALCLK2 appears on the XCK lines and clocks all of the custom chips. The Calibration Module connection code is hard-wired as Hex E2. The Calibration Module has an ID button located externally for detection by the mainframe.

static awareness

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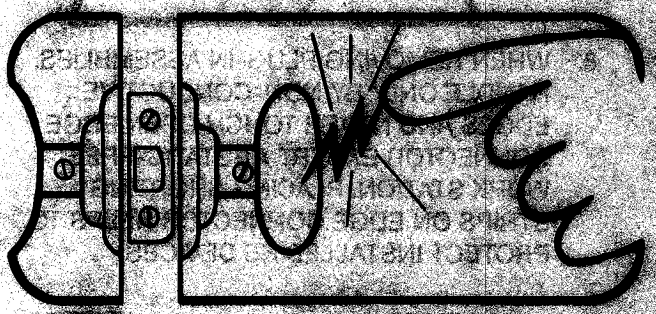
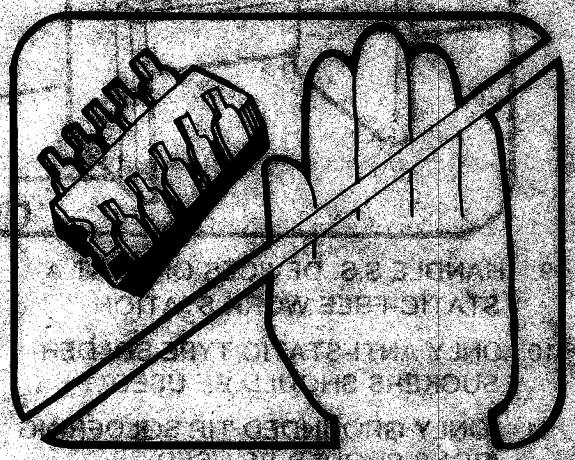


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

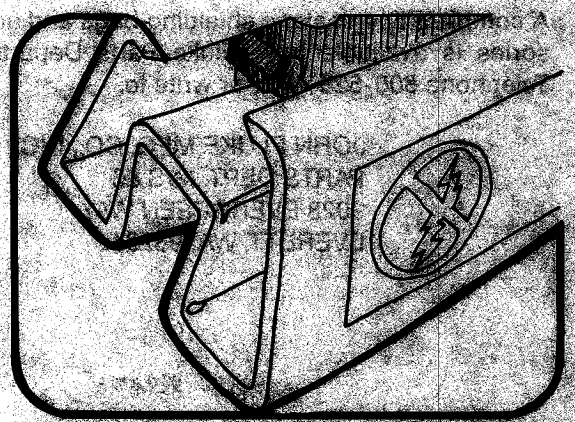
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗".

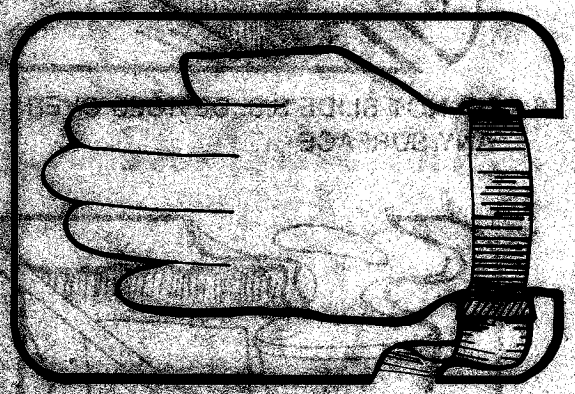
The following practices should be followed to minimize damage to S.S. devices.



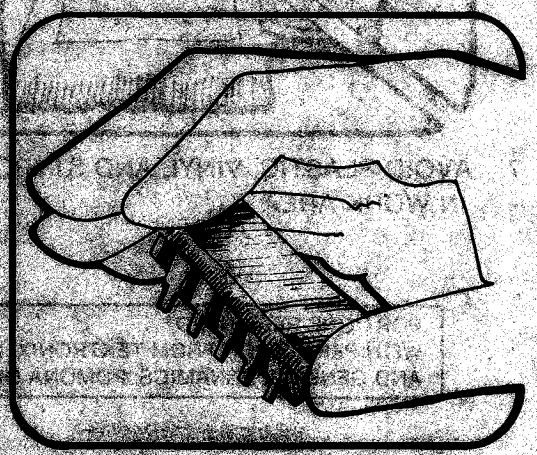
1. MINIMIZE HANDLING



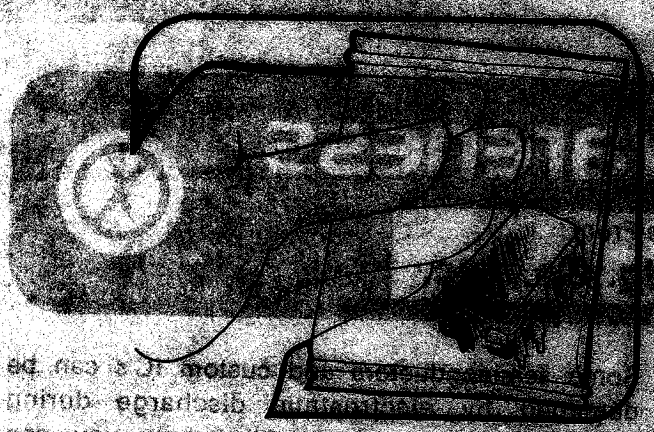
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



4. HANDLE S.S. DEVICES BY THE BODY

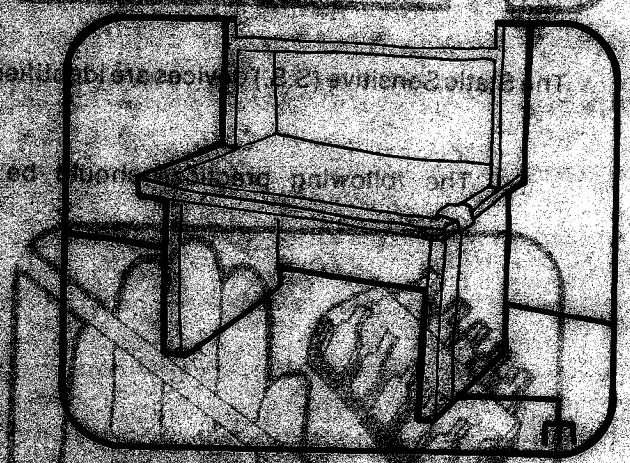


5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT

6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE

7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION

10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

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