Z8 Pod Adapter

for the

Fluke 9000-Series Troubleshooter

May 23, 1984

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This document describes a pod adapter which enables the Fluke 9000-Series Micro-System Troubleshooters to be used for diagnosing Z8-based UUT's. A pod adapter is necessary because no actual pod for the Z8 is available. The adapter described here was originally developed for use with a particular UUT, the Fluke 8840A Digital Multimeter. But its functionality is general enough that it should be useful for many other Z8-based UUT's as well.

The Z8 pod adapter is used in conjunction with a 9000-Series troubleshooter and a 9000A-8048 Interface Pod. The adapter is connected between the 8048 pod and the UUT. It creates Z8-compatible timing signals from the 8048 signals that come from the pod. It also provides I/O pins beyong those of the 8048, so that all input and output functions of the Z8 can be simulated. While the pod adapter does not provide a perfect imitation of an actual Z8 microprocessor, it is quite close. The differences and limitations are detaild in section 5.

1. Conventions Used in This Document

Some I/O ports on the Z8 have the same names as ports on the 8048, even though their functions are unrelated. To avoid confusion between Z8 ports and 8048 ports, we adopt the following convention: Unless explicitly stated otherwise, a mention of an I/O port or a signal refers to the Z8. All references to 8048 ports and signals will be clearly indicated.

An I/O port name such as "Port 2" refers to the port as a whole, i.e., all 8 bits. Individual lines of a port are refered to by their port number and line number. For example, P34 refers to Port 3, line 4. The lines are numbered to correspond to their controlling bits in the Z8. Bit 0 is the least-significant bit.

A nibble is 4 bits of an I/O prot. The low nibble of a port always consists of lines 0-3, and the high nibble consists of lines 4-7.

Signal names, unless otherwise indicated, refer to the Z8 signals. A minus sign at the end of a signal name indicates that the signal is active-low. For example, the signal "DS-" (pronounced "D S bar") is the Z8 data strobe signal and is asserted when it is at a low level.

All addresses and data in this document are expressed in hexadecimal notation.

2. Overview

Figure 1 shows a block diagram of the Z8 pod adapter. About half of the Z8 pins are supported by simple direct connections through the adapter to functionally similar pins on the 8048 pod. The adapter connects the 8048 Bus port directly to the Z8 I/O port 1 pins. Similarly, it connects 8048 I/O Port 1 directly to Z8 Port 2. Finally, the VCC, GND, XTAL1, XTAL2, and RESET- signals are passed directly through the adapter.

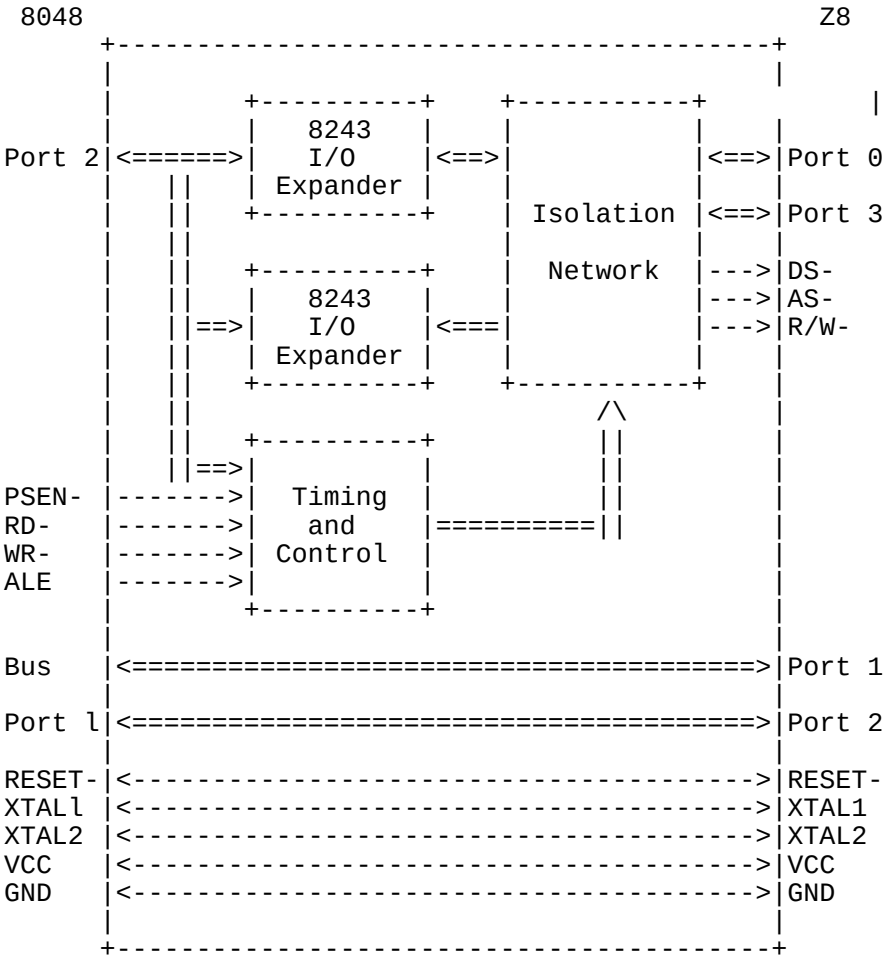


Figure 1. Pod Adapter Block Diagram.

The remainder of the Z8 signals have to be created or derived by circuitry in the pod adapter. Sixteen of these, the I/O lines for Z8 Ports 0 and 3, are provided by an 8243 I/O Expander chip which is controlled by 8048 signals. The final 3 signals are control lines which are derived from 8048 control signals.

A second 8243 I/O Expander provides inputs for sensing the actual levels of I/O and control signals. This sensing capability makes it possible to check the drivability of lines which are connected to logic in the pod adapter. Signals which are directly connected to the pod undergo automatic drivability checking within the pod.

All Z8 pins which connect to logic in the pod adapter pass first through an isolation network which helps to protect the adapter from transients an illegal voltage levels in the UUT. Those Z8 signals which connect directly to equivalent 8040 pins are isolated in the pod itself.

3. Pod Adapter Setup

The pod adapter has a number of modes which affect the way it operates. These modes permit the pod adapter to be used with a fairly wide range of UUT's. They also allow certain drivability checks to be performed which would otherwise be impossible. Before attempting to access I/O ports or external devices, the user must set up the pod adapter modes to conform to the configuration of the particular UUT to which the adapter is connected. All of the pod adapter nodes are controlled by bits in the Mode Register, whose layout is shown in Figure 2. The Mode Register can be written or read at troubleshooter address 2002. The following sections describe the functions of the Mode Register bits.

3.1. Drivability Checking Control (Mode Bit 4)

Each time a new value is written to Port l or Port 2, the troubleshooter automatically senses the levels of the port's I/O lines and compares the actual levels with the values written. Any discrepancy is reported as a drivability error. This automatic drivability checking function is built into the pod. It works correctly on Ports l and 2 even with the pod adapter in place, because those ports are passed directly through the pod adapter without any intervening circuitry. In contrast, Ports 0 and 3 as well as some of the control lines are driven by logic internal to the pod adapter. The troubleshooter cannot directly check the drivability of those lines.

Since drivability checking is an important diagnostic function, the pod adapter contains extra circuitry to permit checking the drivability of Port 0, Port 3, and the DS- and R/W- signals. The extra circuitry allows actua1 output levels to be read back and compared with the desired levels. The checking is not automatic, however; it must be done manually through manipulation of Mode Bit 4.

For normal troubleshooting operations, Mode Bit 4 should be 0. When Mode Bit 4 is 0, reads and writes at addresses 2004-2007 will result in input and output operations on Ports 0 and 3, as described in section 4.

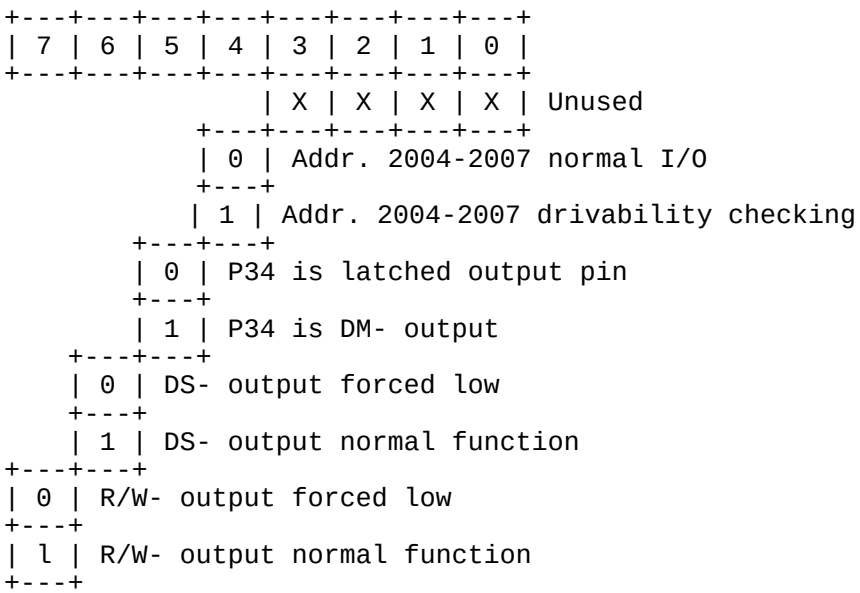


Figure 2. Mode Register Layout.

When values have been written to one or more of these addresses, the actual output levels can be read back after setting Mode Bit 4 to 1. When Mode Bit 4 is 1, previously written values are maintained on the output pins while a separate data path is enabled for reading the actual levels. Here is the procedure for outputting a new value and checking the drivability:

1. Clear Mode Bit 4 to 0 by writing to address 2002.
2. Write desired value to address 2004, 2005, or 2007.
3. Set Mode Bit 4 to 1 by writing to address 2002.
4. Read actual value from the same address as step 2.

Bits whose actual value differs from the desired value correspond to lines that could not be driven.

The attentive reader will notice that the above procedure does not apply to address 2006, the low-order nibble of Port 3. That nibble is restricted by the Z8 hardware to input operations only, so writing to address 2006 is illegal. Without an output capability, drivability checking is meaningless, and it is not provided for the low nibble of Port 3. Instead, a read operation from address 2006 when Mode Bit 4 is 1 will return the actual levels present on the DS- and R/W- control lines, as shown in Figure 3. When used in conjunction with Mode Bits 6 and 7 as described below, this feature permits checking the drivability of the DS- and R/W- lines.

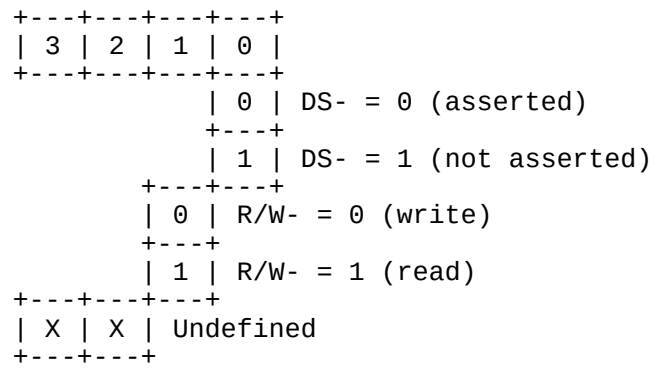


Figure 3. Value from address 2006 when Mode Bit 4 is 1.

To output a new value to Port 0 or Port 3, Mode Bit 4 must be 0. Writes to these ports are illegal when Mode Bit 4 is 1.

3.2. P34 Control (Mode Bit 5)

Pln P34 (Port 3, bit 4) serves a dual function on the Z8. For systems without external data memory or peripherals, it is typically used as a general-purpose latched output pin. For larger systems this pin can be made to output the DM- signal, which serves to distinguish between external program and data memory accesses. The pod adapter supports P34 in both of these roles. The function of P34 is selected by Mode Bit 5. When Mode Bit 5 is 0, P34 serves as a normal output pin which is controlled (along with pins P35-P37) by write operations to address 2007. When Mode Bit 5 is 1, P34 outputs the DM- signal.

3.3. DS- and R/W- Control (Mode Bits 6 and 7)

Mode Bits 6 and 7 should both be set to 1 for normal troubleshooting operations. When cleared to 0, these bits serve to force the DS- (bit 6) and the R/W- (bit 7) signals to the low state. This capability is provided so that the drivability of DS- and R/W- may be checked conveniently. The drivability of these pins is checked by selectively forcing them to 0, then reading their actual levels from address 2006 with Mode Bit 4 set to 1. Note that the quiescent state of each of these signals is 1, so there is no need to be able to force them high.

4. Z8 Operations

The pod adapter is capable of reading and/or writing the Z8 I/O pins as well as memory and I/O devices external to the Z8. All accesses are made by read or write operations from the troubleshooter. The legal troubleshooter addresses and their functions are listed in Table 1. The functions are described in more detail in the following sections.

Table l. Address Space Assignment.

ADDRESS	FUNCTION ADDRESSED
0000-0FFF	External Program Memory
1100-11FF	External Data Memory
2000	Z8 Port 1
2001	Z8 Port 2
2002	Pod Adapter Mode
2004	Z8 Port 0, low nibble
2005	Z8 Port 0, high nibble
2006	Z8 Port 3, low nibble
2007	Z8 Port 3, high nibble
3000-30FF	Executable Pod RAM

4.1. Accessing Port 0

Port 0 is accessed as two independent nibbles, at troubleshooter addresses 2004 (lines P00-P03) and 2005 (lines P04-P07). Each nibble may be configured as 4 input lines or 4 output lines.

Mode Bit 4 must be 0 for normal input and output operations on Port 0. Reading from address 2004 or 2005 configures the corresponding nibble as an input, and reads the levels of its lines. Writing to address 2004 or 2005 configures the corresponding nibble as an output, and latches the data onto its lines. After data has been output to one or both nibbles, the actual output levels can be read back (to check drivability) by setting Mode Bit 4 to 1 and then reading address 2004 or 2005.

If a nibble of Port 0 is to be reconfigured from output mode to input mode, two reads should be performed. The first read will change the mode of the port (turn off the output drivers, etc.), but may return inaccurate data. Subsequent reads will return correct data values. No such special actions are required when changing from input mode to output mode.

4.2. Accessing Port 1

Port 1 is accessed as a single byte, at troubleshooter address 2000. The port as a whole may be configured as 8 output lines or 8 input lines. A write to address 2000 will put the port in output mode and latch the data onto its lines, with drivability checking performed automatically by the troubleshooter. A read from this address will return the data present on the lines of the port, but will not automatically disable the port's output drivers. If Port l has been put in output mode (by a write to address 2000) and is to be changed to input mode, the output drivers must first be turned off by reading from any external program or data memory address; i.e., any troubleshooter

address in the range 0000-0FFF or 1100-11FF. Once this has been done, the actual data may be read from address 2000.

Note that the Z8 uses Port 1 as a bidirectional multiplexed address and data bus when accessing external memory and I/O devices. Direct output and input operations on Port 1 such as those described here will typically be used only with UUT's that do not have such external devices. An external access will remove any previously latched data from the lines of Port 1.

4.3. Accessing Port 2

Port 2 is accessed as a single byte, at troubleshooter address 2001. Each of the port's 8 lines may be independently configured as an input or an output. An output operation is performed by writing the desired data to address 2001. The troubleshooter will automatically perform drivability checking on the lines of Port 2. An input operation can be performed by reading from address 2001. Lines of Port 2 which are to be used as inputs first must be configured to the input mode by outputting 1's to them.

4.4. Accessing Port 3

Port 3 is accessed as two separate nibbles, at addresses 2006 (P30-P33) and 2007 (P34-P37). Lines P30-P33 may be used only as inputs, and lines P34-P37 may be used only as outputs. Mode Bit 4 must be 0 when accessing Port 3.

After writing data to P34-P37, the drivability of those lines may be checked by setting Mode Bit 4 to 1 and then reading address 2007. The value returned will contain the actual levels on pins P34-P37. Any differences between the actual levels and the values written are symptomatic of drivability problems.

4.5. Accessing External Program Memory

Program memory external to the Z8 (in the UUT) may be read at addresses 0000 to 0FFF. This memory is considered to be read-only, and it cannot be written by the troubleshooter.

Only the least-significant 8 bits of the address are transmitted by the pod adapter; the high-order address bits are discarded. Because of this, reads at (for example) 0057, 0l57, 0257, etc. will all access the same program memory location. Different 256-byte pages of program memory can be selected by outputting the high-order address bits to Z8 Port 0. Either 4 or 8 bits of high-order address may be output, depending on the address range and decoding logic of the UUT. If the UUT decodes only a 12-bit address, the upper 4 bits should be written to the lower nibble of Port 0 (troubleshooter address 2004). If the UUT decodes a 16-bit address, the highest 4 bits should be written to the upper nibble of Port 0 (troubleshooter address 2005) and the next 4 bits should be written to the lower nibble of Port 0 (troubleshooter address 2004).

As an example, suppose the UUT contains 4K bytes of external program memory (12-bit address decoding). The following steps would be

used to read the byte at location 0457:

```
WRITE @2004 = 4 (select page 4)
READ @0457 (read the data)
```

In this example, the address given in the read operation could have been 0057 with the same result, since the high-order address bits are discarded. However, specifying the actual address is recommended to avoid confusion.

Accesses to external program memory use Z8 Port 1 as a multiplexed address and data bus, with address and data strobes being output via the AS- and DS- pins, respectively. Port 0 is used to output the high-order address bits.

4.6. Accessing External Data Memory

Troubleshooter addresses 1100-11FF are used to access data memory in the UUT. This address space is considered to be readable and writable. It typically will consist of a mixture of RAM and memory-napped I/O devices. If the data memory address space in the UUT is larger than 256 locations, the high-otder 4 or 8 address bits must be output via Port 0 before the access is made. The procedure is exactly as described in section 4.5 for program memory fetches.

As an example, the following steps would be used to write the value 38 to data memory location 07CA, assuming 12-bit address decoding:

```
WRITE @2004 = 7 (select pape 7)
WRITE @11CA = 3B (write the data)
```

Aceesses to external data memory use Z8 Port 1 as a multiplexed address and data bus, with address and data strobes being output via the AS- and DS- pins, respectively. Port 0 is used to output the high-order address bits. If pin P34 is configured as the DM- signal, it will be asserted low during the data transfer. The R/W- signal is asserted low during a write data transfer.

4.7. Sensing the Serial Input Pin

Input line P30 can serve as a serial input on the Z8. The pod adapter connects the 8048 test input T1 to this line to facilitate sensing the level of the serial input. The P30 input can be observed by issuing the READ STS command to the troubleshooter. Status bit 2 will contain the level of the serial input line. When running programs in the pod RAM (see section 4.8), the 8048 instructions "JT1" and "JNT1" may be used to branch depend1ng on the level at this input.

Of course, line P30 also can be read along with lines P3l-P33 by reading troubleshooter address 2006, as explained in section 4.4.

4.8. Running Programs in the Pod RAM

Machine language programs up to 256 bytes in length can be loaded into pod-resident RAM and executed using the Run UUT command. The pod RAM is accessed through write and read operations at troubleshooter addresses 3000-30FF. During execution, the pod RAM will be treated as

though it were at microcomputer addresses 0000-00FF.

There are a few very important caveats regarding the execution of programs in the pod RAM. First and most important is the fact that the programs must be written in machine language for the 8048, not the Z8. The programs are executed by the 8048 in the pod, and it is not "aware" that the adapter is making its external signals appear to be those of the Z8. Even with the pod adapter in place, it is not possible to execute Z8 instructions.

The Z8 I/O ports are manipulated from an 8048 program through operations on 8048 I/O ports. Table 2 shows the correspondence between 8048 I/O ports and Z8 ports.

Port 1 (corresponding to the 8048 Bus) may not be used as a static I/O port during a Run UUT operation, because fetched instructions are transferred over its lines.

The troubleshooter resets the 8048 at the beginning of the Run UUT operation. The reset places all I/O ports in the input mode. There must be instructions at the beginning of the 8048 program to configure the I/O ports before they can be used for outputting data. This applies also to the Adapter Mode Register; it must be set to the appropriate value by 8048 instructions before the other I/O ports can be accessed.

When the Run UUT operation is terminated, the troubleshooter resets the 8048 again. The user must reconfigure the Adapter Mode Register and the I/O ports through troubleshooter commands before proceeding.

5. Limitations

When used together with an 8048 pod, the Z8 pod adapter provides most of the functionality of an actual Z8 microprocessor. The adapter is able to control all Z8 output lines, sense all Z8 input lines, and access the entire Z8 external address space. The adapter is, however, somewhat different from an actual Z8 in terms of input loading, output drive capability, clock oscillator characteristics, and external access timing. The differences are discussed in the following sections.

5.1. Input Loading

Input loading on all ports is practically insignificant (a few microamperes) for both the Z8 and the pod adapter, with one exception. Port 2 in the adapter contains pull-up resistors which can leak up to 500uA. into an input at the logic 0 level. For most UUT's this leakage will be acceptable, since it represents less than one third of a standard TTL load.

5.2. Output Drive Capability

The Z8 microprocessor can source 250uA. at an output high level of 2.4V., and can sink 2.0mA. at an output low level of 0.4V. The pod adapter comes very close to meeting this drive capability on Ports 0 and 3, and greatly exceeds it on Port 1, AS-, DS-, and R/W-. The only adapter port with significantly less drive than the actual Z8 is Port 2. On Port 2, the adapter can source only 40uA. at 2.4V., and can sink only 1.6mA. at 0.6V.

Table 2. I/O Port Correspondence.

Z8 PORT	8048 PORT	INSTRUCTIONS

Port 0, low nibble	8243 Expander Port 4	MOVD A,P4
		MOVD P4,A
		ANLD P4,A
		ORLD P4,A

Port 0, high nibble	8243 Expander Port 5	MOVD A,P5
		MOVD P5,A
		ANLD P5,A
		ORLD P5,A

Port l	8048 Bus	(Do not use)
Port 2	8048 Port 1	IN A,P1 OUTL P1,A ANL P1,#data ORL P1,#data

Port 3, low nibble	8243 Expander Port 6	MOVD A,P6
		MOVD P6,A
		ANLD P6,A
		ORLD P6,A

Port 3, high nibble	8243 Expander Port 7	MOVD A,P7
		MOVD P7,A
		ANLD P7,A
		ORLD P7,A

Serial Input (P30)	8048 T1 Input	JT1 addr JNT1 addr
Adapter Mode Register	8048 Port 2	IN A,P2 OUTL P2,A ANL P2,#data ORL P2,#data

5.3. Clock Oscillator Characteristics

The pod adapter utilizes the clock circuit in the 8048 pod to generate timing signals. The adapter adds an extra length of cable between the pod and the UUT, increasing the stray capacitance associated with the crystal circuit. While the pod's clock circuit has been designed to be relatively insensitive to stray capacitance effects, it is possible that the crystals in some types of UUT may fail to oscillate with the

adapter in place. The adapter has provisions for installing a crystal directly on the adapter circuit board, thus bypassing the extra cable which runs from the adapter to the UUT.

UUT's which drive the XTAL1 input with a TTL signal instead of using a crystal can be expected to function properly with the adapter. Those which utilize the XTAL2 output to drive TTL loads may not work. The XTAL2 signal provided by the pod and passed through by the adapter is not truly TTL compatible, and the oscillator may fail to run if XTAL2 is loaded by one or more TTL gates. This output has been successfully used to drive a CMOS circuit, however.

5.4. External Access Timing

External program and data memory accesses from the pod adapter are slower than the equivalent Z8 accesses by a factor of about 2.5, for a given crystal frequency. A Z8 running at 8MHz. completes a memory cycle in 750ns., while the adapter at the same clock rate has a memory cycle of 1.875us. Because of the lower speed, the adapter places much less stringent demands on external memory devices. External accesses from the pod adapter should be expected never to fail due to timing differences.

Figures 4, 5, and 6 contain detailed timing diagrams for the program memory fetch, data read, and data write cycles. Each figure shows the timing produced by the pod adapter as well as that produced by an actual Z8 microprocessor. These diagrams are drawn to a common scale for easier comparison.

As seen from the timing diagrams, the major qualitative difference introduced by the adapter involves the DM- and R/W- signals. These signals are valid on the Z8 for what essentially amounts to the entire memory cycle. The adapter, however, asserts these signals only during the Data Strobe (DS-) pulse. This difference should rarely if ever be a problem, especially since the cycle as a whole is so much slower than the Z8 cycle. It will never affect the program memory read cycle, because the DM- and R/W- signals are not asserted during program memory fetches.

A final observation from the timing diagrams is that the 9000-series probe synchronization pulses are valid for both address and data transfers.

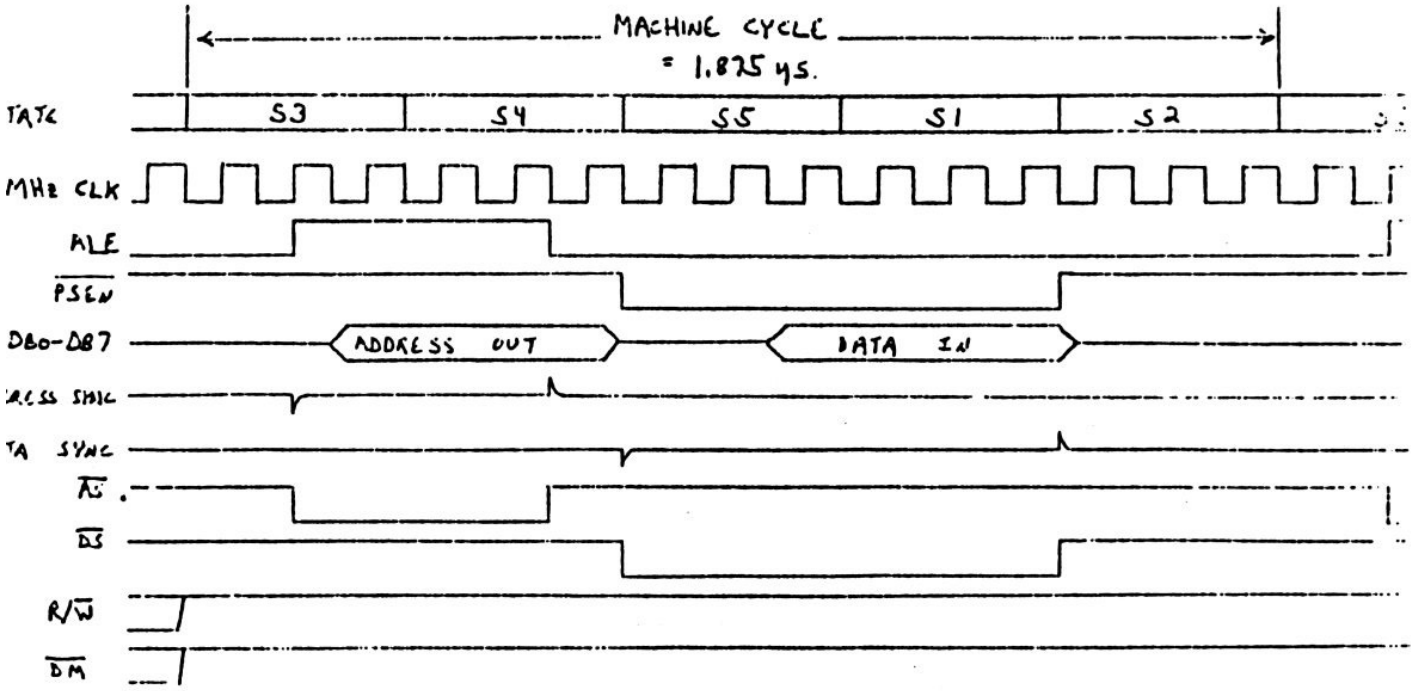


FIG. 4a. PROGRAM MEMORY FETCH TIMING FOR 8048 POD WITH ADAPTER

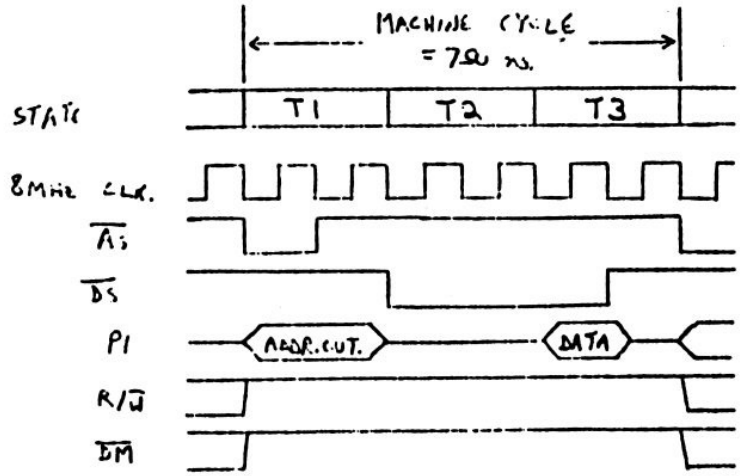


FIG. 4b. PROGRAM MEMORY FETCH TIMING FOR Z8

NOTE: THESE DIAGRAMS ARE DRAWN TO THE SAME TIME SCALE. THE Z8 IS MUCH FASTER THAN THE 8048, FOR A GIVEN CLOCK FREQUENCY.

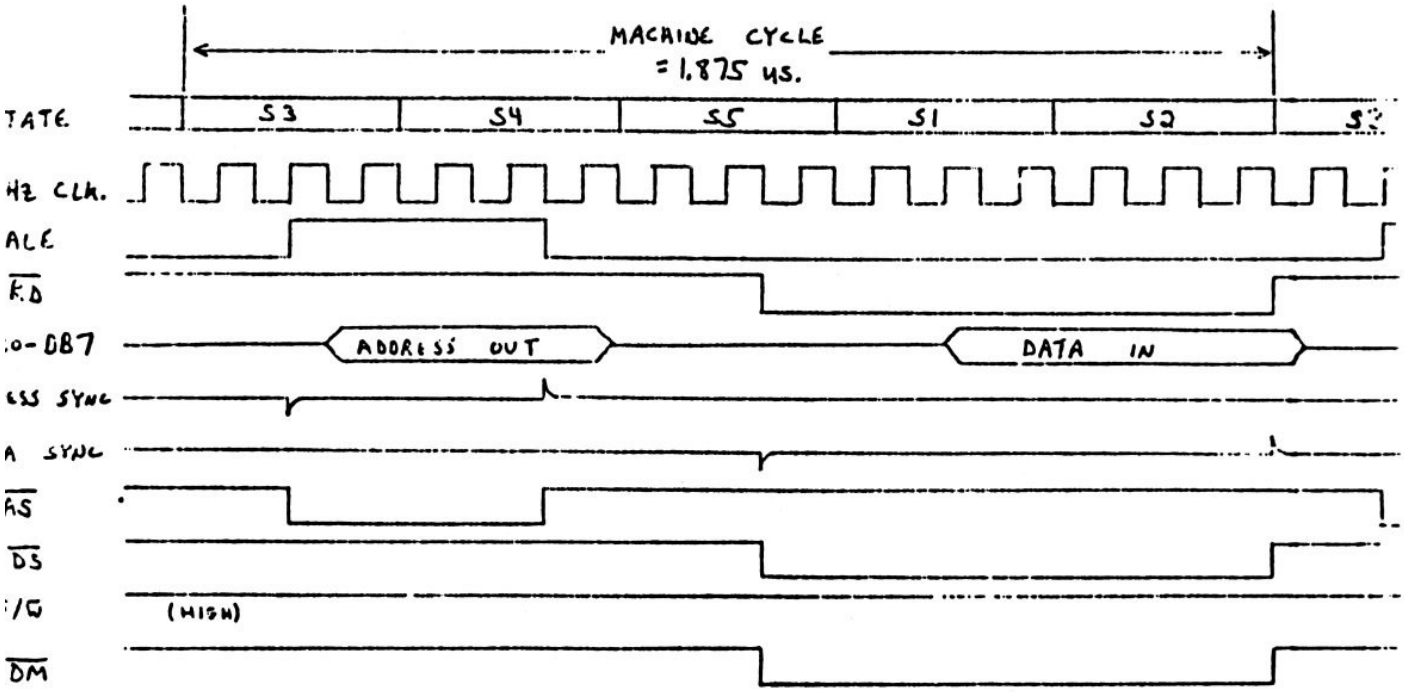


FIG. 5a. DATA READ TIMING FOR 8048 POD WITH ADAPTOR

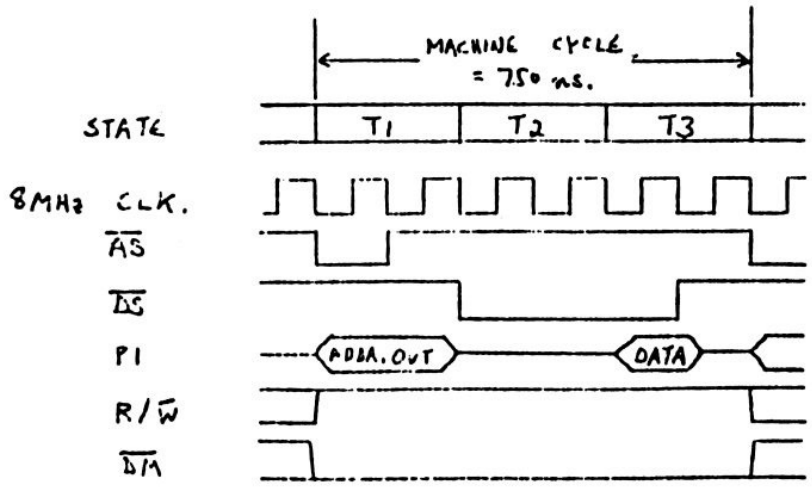


FIG 5b. DATA READ TIMING FOR 28

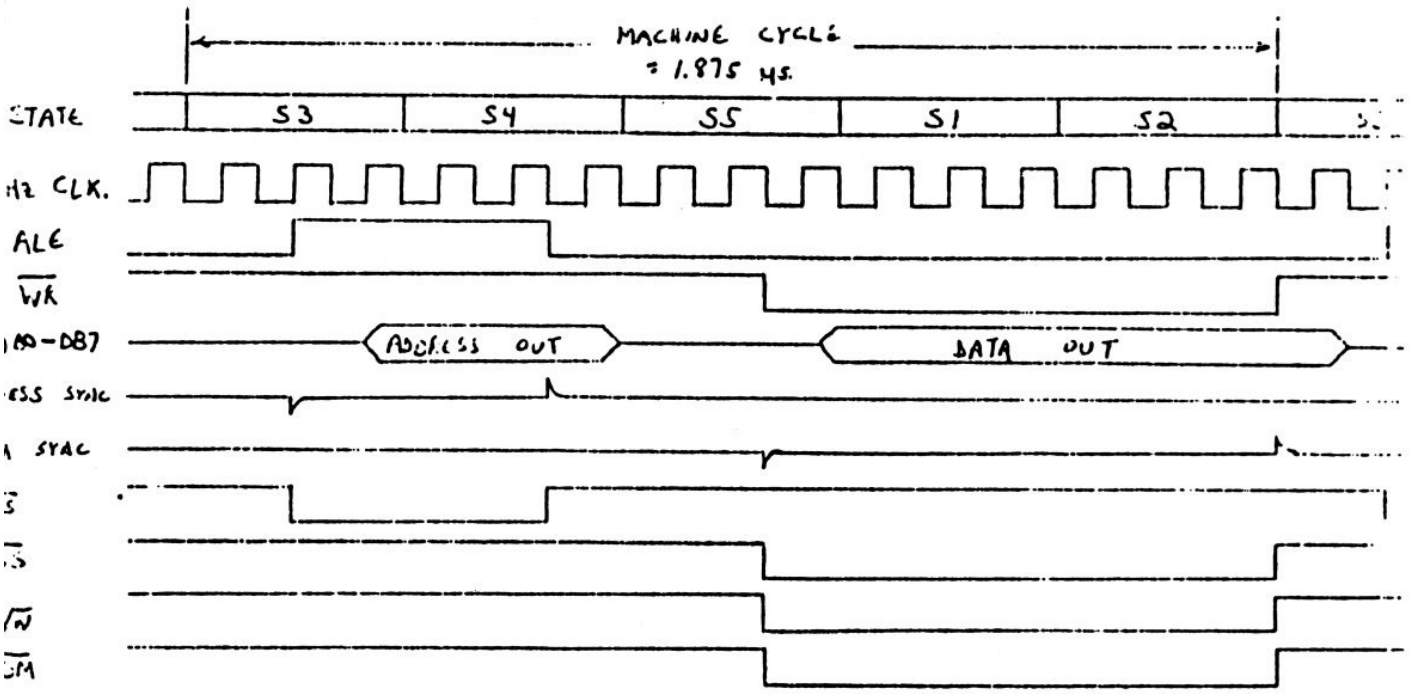


FIG. 62. DATA WRITE TIMING FOR 8048 POD WITH ADAPTOR

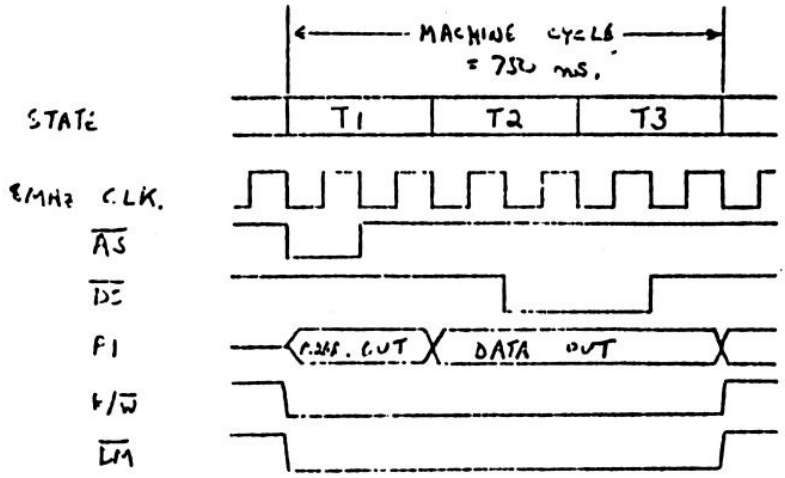


FIG 63. DATA WRITE TIMING FOR 28

APPENDIX A

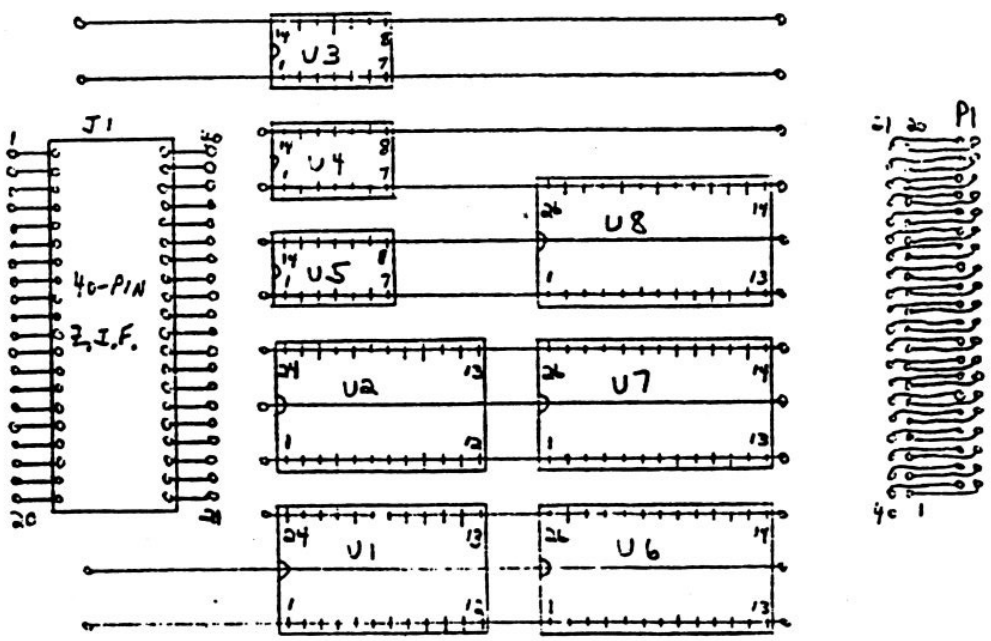
Schematic Diagrams

1. SLIDE IC'S LEFT OR RIGHT IF NECESSARY.

2. PUT A .22uF DECOUPLING CAPACITOR FROM Vcc TO GND NEAR EACH IC.

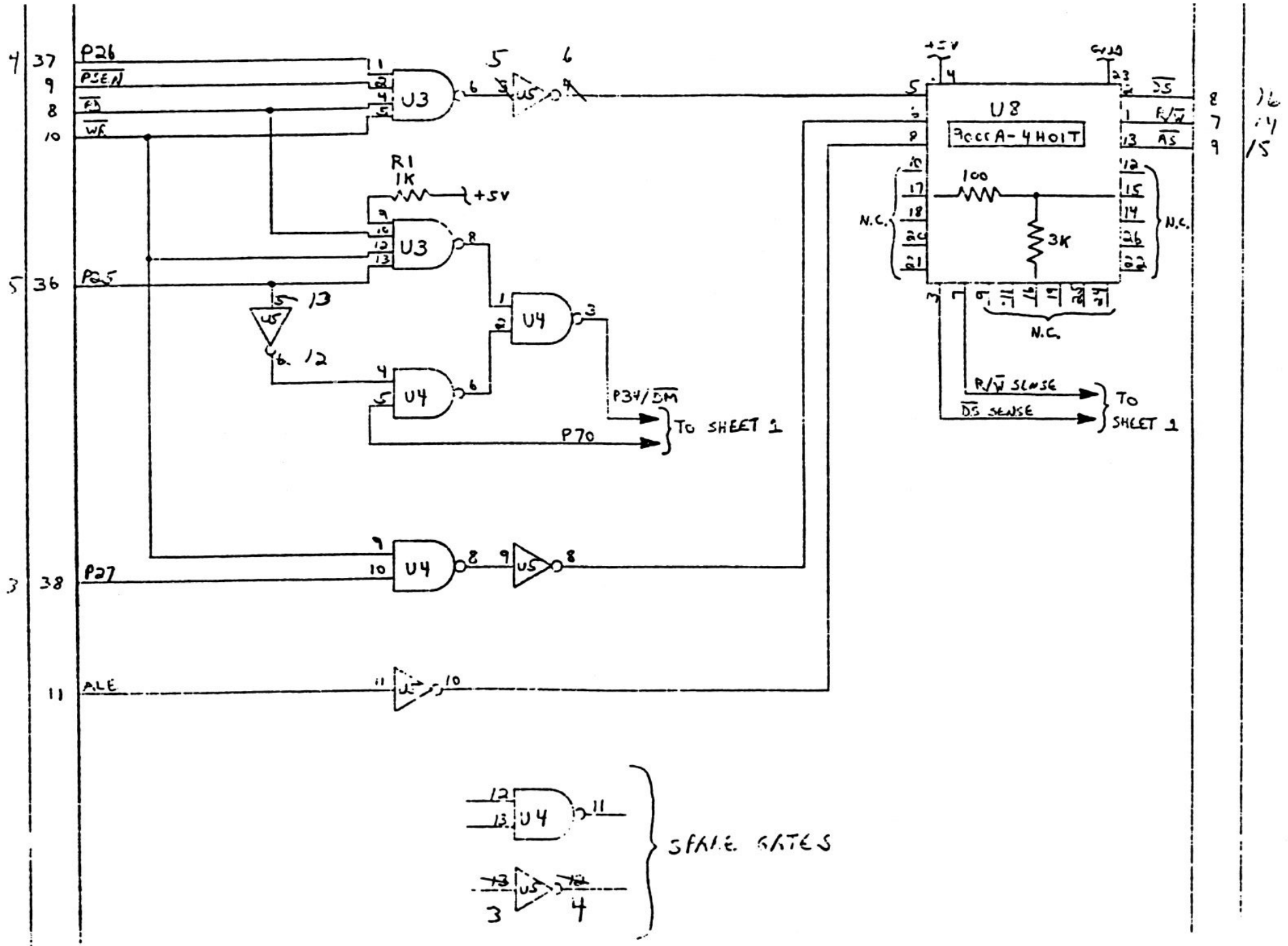
3. IF NO 24-PIN SOCKETS ARE AVAILABLE, USE 22-PIN SOCKETS FOR U6, U7, AND U8.

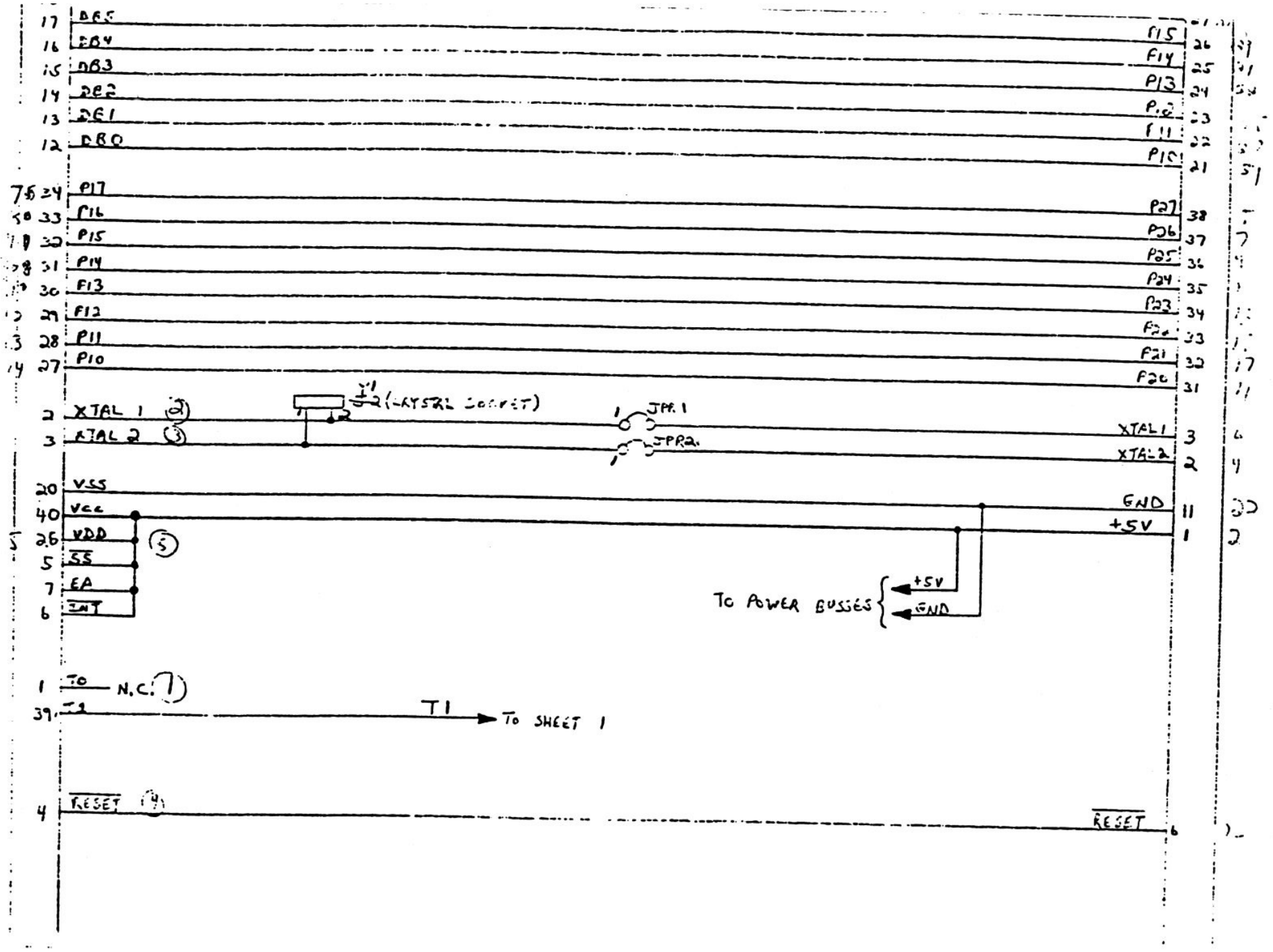
4. USE WIRE-WRAP SOCKETS FOR ALL IC'S.

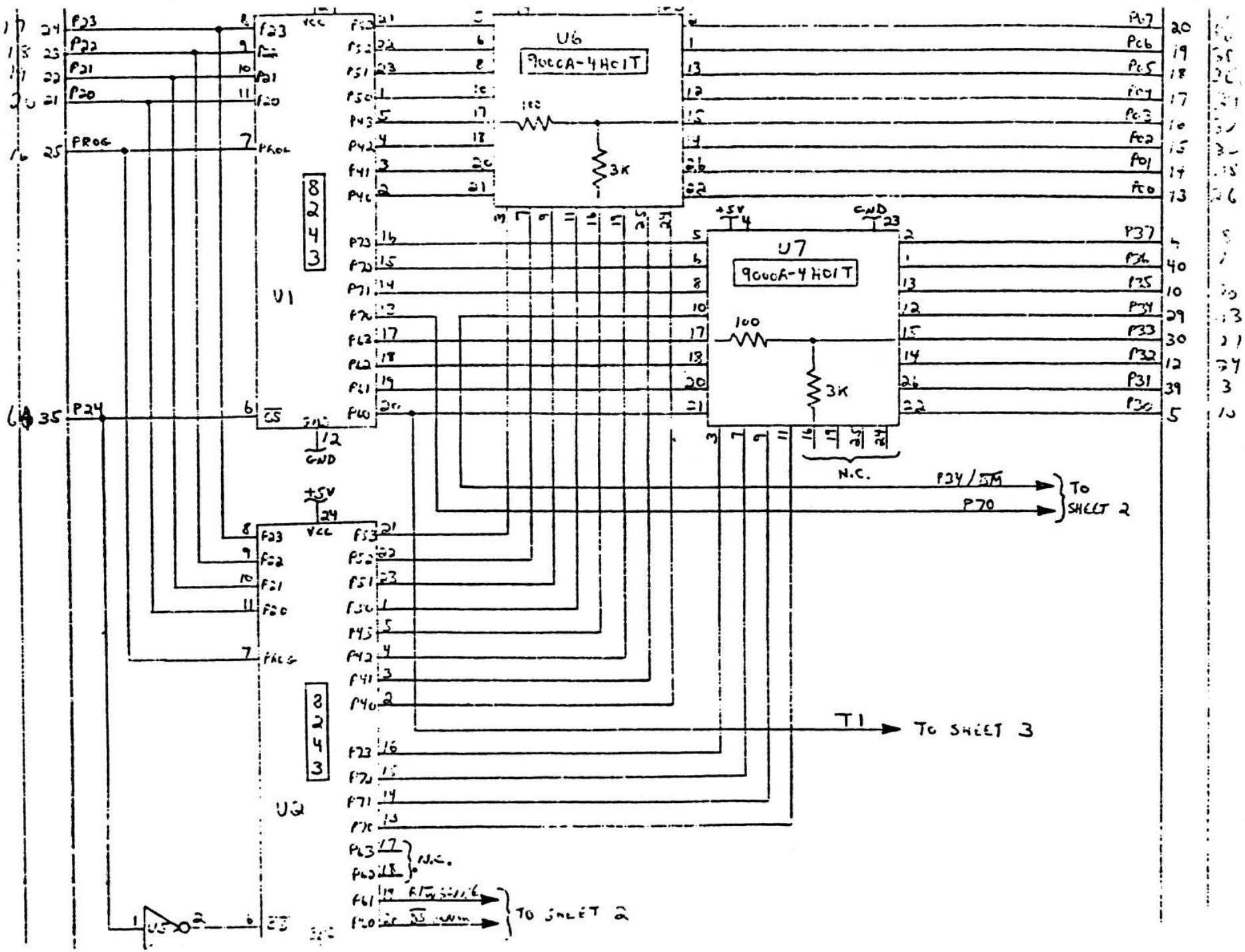


COMPONENT SIDE

TCCCA-20e PC3 ADAPTOR KIT


P26
PSEN
RD
WR
P25
P27
ALE
37
9
8
10
36
38
11
U3
U4
U5
R1
1K
+5V
13
12
P34/DM
P70
TO SHEET 1
U8
P8088A-4 HOIT
100
3K
N.C.
R/W SENSE
DS SENSE
SPARE GATES


DB5
DB4
DB3
DB2
DB1
DB0
P17
P16
P15
P14
P13
P12
P11
P10
XTAL 1
XTAL 2
VSS
VCC
VDD
SS
EA
INT
Y1 (CRYSTAL SOCKET)
JPR 1
JPR2
P15
P14
P13
P12
P11
P10
P27
P26
P25
P24
P23
P22
P21
P20
XTAL1
XTAL2
GND
+5V
TO POWER BUSSES
+5V
GND
TO N.C.
T2
T1
TO SHEET 1
RESET
RESET


U6
90LCA-4HC1T
100
3K
U7
90LCA-4HC1T
100
3K
+5V
GND
N.C.
U1
U2
8243
P23
P22
P21
P20
PROG
P24
P34/SM
P70
To SHEET 2
T1
To SHEET 3
P63
P62
N.C.
P61
P60
To SHEET 2