SECTION 12 GLOSSARY

GLOSSARY

SIGNAL NAME	DESCRIPTION
10 ns(L)(H)	The Trigger's 10 ns clock to the counter portion of the counter/timer.
ACARD(L)	The 18-Channel's A-side control signal indicating that storage should occur on this card rather than a subsequent chained card.
ACC OUT(H)	The 18-Channel's A-side chaining clock signal used by the Data Chain Interface.
ACH 0(H)(L)-ACH 8(H)(L)	The 18-Channel's differential data from the A probe.
A CLK0(H)	The 18-Channel's A-side master sample clock derived from the selected timebase T1, T2F, or T2L.
A CLK1(H)	The 18-Channel's clocking signal for the probe data latches in the Data Chain Interface.
ACORO(L)	The 18-Channel's A-side correlation data readback signal line from the acquisition RAMs.
ACQ RUN(L)	The Trigger's phase delayed signal used to start the acquisition after starting the trigger.
A FORCE STR(L)	The 18-Channel's A-side signal forcing storage of data (in the Data Chain Interface) into acquisition RAM.
A HOLDOFF(H)	The 18-Channel's A-side global word recognizer holdoff signal line.
ALE(H)	The Control Processor's address latch enable signal used to latch address information on the processor's multiplexed address/data bus.
A MAP CLK(H)	The 18-Channel's A-side memory address pointer clock signal line.
APB CLK(H)	The 18-Channel's A-side clock signal used during probe programming and probe data readback.
A PROBE DF(H)	The 18-Channel's A-side probe data readback signal line from each probe.
APROBE DT(H)	The 18-Channel's A-side signal for control of a programmable probe (not currently used).
APROBE R(L)/W(H)	The 18-Channel's A-side control signal used for probe programming and probe data readback.
A SLO CLK(H)	The 18-Channel's A-side slow clock detector signal line.
ATB(H)	The Trigger's asynchronous timebase output signal.
AT RESET(H)	The Trigger's signal generated when Trigger is attempted; used to generate system reset.
A WR PULSE(L)	The 18-Channel's A-side acquisition RAM write signal line.
BACK UP(L)	The Control Processor Board's nonvolatile memory select signal.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
BATT TEST(H)	The Control Processor Board's nonvolatile memory battery-voltage signal line indicating battery voltage level.
BCARD(L)	The 18-Channel's B-side control signal indicating that storage should occur on this card rather than a subsequent chained card.
BCC OUT(H)	The 18-Channel's B-side chaining clock signal used by the Data Chain Interface.
BCH0(H)(L)-BCH8(H)(L)	The 18-Channel's differential data from the B probe.
B CLK0(H)	The 18-Channel's B-side master sample clock derived from the selected timebase T1, T2F, or T2L.
B CLK1(H)	The 18-Channel's clocking signal for the probe data latches in the Data Chain Interface.
BCORO(L)	The 18-Channel's B-side correlation data readback signal line from the acquisition RAMs.
B FORCE STR(L)	The 18-Channel's B-side signal forcing storage of data (in the Data Chain Interface) into acquisition RAM.
B HOLDOFF(H)	The 18-Channel's B-side global word recognizer holdoff signal line.
BLANK(L)	The Display Board's video blanking signal used to disable the video output at the end of each raster line and during vertical retrace.
B MAP CLK(H)	The 18-Channel's B-side memory address pointer clock signal line.
BMREQ(L)	The I/O Processor Board's buffered memory request signal line; output goes active to indicate that the address bus holds a valid address.
BPB CLK(H)	The 18-Channel's B-side clock signal used during probe programming and probe data readback.
BPROBE DF(H)	The 18-Channel's B-side probe data readback signal line from each probe.
BPROBE DT(H)	The 18-Channel's B-side signal for control of a programmable probe (not currently used).
BPROBE R(L)/W(H)	The 18-Channel's B-side control signal used for probe programming and probe data readback.
B SLO CLK(H)	The 18-Channel's B-side slow clock detector signal line.
BUF(L)	The Display Board's buffer enable signal used when the I/O Processor writes to the Display Board through the I/O P-Display RAM Interface.
BUF STR 1(H), 2(H)	The Trigger's buffered store signals for timebase 1 and 2.
B WR PULSE(L)	The 18-Channel's B-side acquisition RAM write signal line.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
C0(H)-C2(H)	Sent from the I/O Processor to produce a sequential count for scanning the LED/PT matrix.
CA0(H)-CA2(H)	The Control Processor's address lines used when addressing linked circuitry.
CAS(L)	The Control Processor Board's column address strobe signal used to latch column data into the Display RAMs.
CC0*(H), CC1*(H)	The 18-Channel's A- and B-side chaining clocks from the Data Chain Interface on present card to the next 18-Channel Acquisition card in the chain. The asterisk denotes a letter that changes when moved from acquisition slot to slot.
C CLK(H)	The Display Board's character clock signal used to latch character data from the Display RAM into the character ROM latch.
CCOR1*(H), CCOR2*(H)	The 9-Channel's chain correlation data lines into this 1240D1 from the upper (previous in chain) 1240D1. The asterisk denotes a letter that changes when moved from acquisition slot to slot.
CCOUT(H)	The 9-Channel's chain clock out destined for lower 1240D1's in the system.
CHAIN(L)	The 9-Channel's signal causing the storage of data on lower 1240D1's in the system.
CHAIN CLOCK IN(H)	The incoming acquisition clock from upper (previous in chain) acquisition board in the memory chain.
CHAIN SEL(L)	The 18-Channel's enable for incoming chain clocks.
CHAR(L)	The Display Board's character signal indicating the display is in character mode.
CLK 0(H)	The 9-Channel's master sample clock derived from the selected timebase T1, T2F, or T2L.
CLK 1(H)	The 9-Channel's data hold register clock.
CLK 2(H)	The 9-Channel's glitch hold register clock.
CLK DIS(L)	The 18-Channel's enable for ordinary storage clocks.
CLR MAP(H)	The 9-Channel's clear memory address pointer signal derived from Control Processor control lines; used when clearing MAP counters and load counter for sequential word and glitch values.
CODE(L)	Generated by the Control Processor's Select Decode circuitry when accessing the lower bank of Control Processor ROMs.
COM(H)	The 18-Channel's common serial data readback signal line from the acquisition RAM circuitry.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
COMM(L)	The communication pack select line from the I/O Processor to the installed COMM pack; used to enable the pack's communication I.C.
COMPOSITE VIDEO OUT(H)	Carries the composite video signal from the CRT Drive Board to the rear panel output connector.
COR 1(H), COR2(H)	The Trigger's correlation data from timebases 1 and 2, respectively, to the acquisition circuitry.
CORR 1 RB A,B,C(L)	The Trigger's timebase 1 correlation readback.
CORR 2 RB(L)	The Trigger's timebase 2 correlation data readback.
COR D(H)	The 9-Channel's correlation data signal carrying correlation information destined for the data half cycle of the acquisition storage RAMs.
COR G(H)	The 9-Channel's correlation glitch signal carrying correlation information destined for the glitch half-cycle of the acquisition storage RAMs; not used when glitches are being stored.
C/Q(H)(L)	The acquisition board probe clock/qualifier signals; used in the generation of T clocks and Q qualifiers.
CQ1(L)-CQ3(L)	The 18-Channel's clock and qualifier generation programming strobe.
CQ GEN(H)	The 9-Channel's signal derived from Control Processor control lines; used as a write strobe when loading clock qualifier generation values.
CRD(L)	The Control Processor's read signal used when communicating with linked instrument circuitry.
CROM(L)	The COMM pack ROM select signal from the I/O Processor to the installed COMM pack.
CS0(L)-CS3(L)	Chip select signals from the Control Processor to the currently installed RAM pack; used to select individual memory I.C.'s within the pack.
CSYNC(H)	Composite synchronization signal from the Display Board to the CRT Drive's Composite Video Amplifier; used to generate the rear panel Composite Video Out signal.
CT EN(H)	The Trigger's sequence signal enabling events to counter/timer.
CT IN(L)(H)	The Trigger's counter/timer input signal to load the event into the counter/timer.
CT INHIBIT(H)	The Trigger's inhibit signal to the counter/timer; asserted after a trigger occurs.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
CT READ 1(H), 2(H)	The Trigger's counter/timer read 1 and 2 signals derived from Control Processor control signals; used for reading counter/timer.
CT RESET(L)(H)	The Trigger's command signal to reset the counter/timer.
CT STB(H)	The Trigger's counter/timer strobe derived from Control Processor control signals; used for loading C/T vector RAM.
CT OUT(L)	The Trigger's signal indicating counter/timer is at terminal count.
CT TRIG(L)	The Trigger's control line used to select/enable the counter/timer as the Trigger source.
CUR(H)	The Display Board's timing diagram cursor data signal line; data indicates the horizontal position of the timing diagram cursor.
CURSOR SELECT(L)	The Display Board's ciruitry select line used when the I/O Processor writes to the cursor attribute register.
CWR(L)	The Control Processor's write signal used when communicating with linked instrument circuitry.
DATA 0(L)	The 9-Channel's signal derived from Control Processor control signals; used by the Storage RAM Data Readback circuitry when reading from RAM.
DATA OUT(H)	The 9-Channel's data out line carrying serial data from the Front End Hybrid serial control registers.
DIAG(L)	Generated by the Control Processor's Select Decode circuitry when accessing the upper bank of Control Processor ROMs.
DIV2(H)	The 9-Channel's signal derived from Control Processor control signals; used when glitch data is not stored.
DELAYED BUF STR 1(H)	The Trigger's buffered store 1 signal (delayed).
DELAYED QUAL CLK2(H)	The Trigger's delayed qualified timebase 2 signal used for trigger control.
DEMUX(H)	The Trigger's control signal used to enable the T2 Demux mode circuitry.
DEN(L)	The Control Processor's data enable signal that activates the bidirectional Instrument Data Buffer. The enable signal prevents bus contention while the 8088 is transferring data on the AD data bus lines.
DMEM(L)	The display memory select signal from the I/O Processor to the Display Board circuitry; used to indicate the I/O Processor is ready to access the Display RAM.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
DREG(L)	The display register signal from the I/O Processor to the Display Board; used to indicate the I/O Processor is ready to write to display registers.
DT1(H), DT2(H)	The Trigger's delayed sample clocks 1 and 2 for sequence timing.
DT1, DT2 RET(H)	The Trigger's delayed return signal for T1 and T2.
DT(H)/R(L)	The Control Processor Board's data transmit/receive signal; used to control the direction of data on the 8088 CPU bus, the Dynamic RAM data bus, and the nonvolatile memory data bus.
ECL STK STB(H)	The Trigger's stack strobe signal; serves as a load strobe for the counter/timer.
ECL TH	The ECL level threshold voltage (approximately 3.6 V).
ETI OFF(H)	The Trigger's control line used to disable the external trigger input.
ETO(H)	The Trigger's signal indicating the current status of the external trigger out latch (for processor readback).
ETO LATCH(H)	The Trigger's control line used to enable latching of the external trigger out.
ETO OFF(H)	The Trigger's control line used to disable the external trigger out.
FLAGS(L)	The 9-Channel's signal derived from Control Processor control lines; used when reading the no-clock (flag) register.
FO(H)	The 9-Channel's filled once signal; used to locate the oldest/youngest data boundary.
GA SWR(H)	The gate arrray (front end hybrid) or sequence word recognizer programming select line.
GATE(L)	The Display Board's blanking signal used by the Timing Diagram ROM when generating tick marks.
GE(L)	The Trigger's global event signal.
GF0(H)-GF3(H)	The Trigger's control signals that specify the global filter values.
GF 10ns(L)	The Trigger's control signal set when the global filter clock is set to 10 ns.
GF=1(H)	The Trigger's control signal set when global filter= 1 is specified.
GF=1=LVL(H)	The Trigger's control signal set true when the user specifies global filter= 1 and level mode (as opposed to edge mode) is being used.
GF<3(H)	The Trigger's control signal set when the global filter value specified is less than 3.
GF CT EN(H)	The Trigger's control signal used to enable the global filter as the input to the counter/timer.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
GF DT1(L), DT2(H)	The Trigger's control signals set when the global filter clocks are T1 and T2, respectively.
GF EDGE(H)	The Trigger's control signal set to use the edge mode (as opposed to the level mode) in the global filter.
GF OUT(H)	The Trigger's signal indicating the global filter has been satisfied.
GF RESET(L)	The Trigger's control line used to select/enable global filter out to be the Reset source.
GF TRIG(L)	The Trigger's control line used to select/enable the global filter out to be the Trigger source.
GGR(H)	The acquisition board's global glitch recognizer signal; when active it indicates the recognition of current global glitch.
GLITCH(H)	The Display Board's timing diagram glitch data signal carrying serial data to the Timing Diagram ROM.
GWR(L)	The acquisition board global word recognizer signal; when active it indicates the recognition of current global word.
GWR HO(H)	The 18-Channel's global word recognizer hold off signal line; derived from Control Processor control signals.
HALF BYTE(H)	The 9-Channel's signal indicating data position on half-cycle RAM write operations.
HD(L)	The Display Board's horizontal drive signal that synchronizes circuitry to the CRT Drive Board's horizontal sweep.
HIGHLIGHT(L)	The Display Board's character attribute signal specifying light characters on a shaded background.
HIGH SELECT(L)	The Display Board's circuitry select line used when the I/O Processor writes to the vertical scrolling registers.
HOLD(H)	The 9-Channel's signal used to hold half-cycle of data during RAM write operations.
IBS1(L)-IBS5(L)	Instrument board select signals from the Control Processor to linked instrument circuitry; used to select specific instrument functions.
INIT(H)	The Trigger's signal used for part of system initialization prior to the acquisition cycle.
INTC(L)	The installed COMM pack's interrupt signal line to the I/O Processor; used to indicate communication with the instrument is desired.
IO(H)	The I/O Processor Board's in-out signal to the Bidirectional Data Buffer; used to enable the communication link between the processor and other functional blocks operating on the ND data bus.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
IO(H)/M(L)	The Control Processor Board's Input Output/Memory signal; used to specify that the current 8088 address is for either a memory device or an input-output device.
IRQ(L)	The I/O Processor's interrupt request signal activated when a COMM pack, the Control Processor, or the display requests an interrupt.
IRST(H)	Interrupt reset signal from the I/O Processor to the Control Processor; resets the Control Processor when a master system reset is performed.
IT CLK(H)	The Trigger's sequential signal used to clock the iteration counters.
ITER RAM(L)	The Trigger's load signal for control RAMs containing sequential iteration count.
IWAIT(L)	The interrupt wait signal from the display circuitry to the I/O Processor; used to prevent the Z80 CPU from accessing display memory until the Display Board is finished accessing it.
KA(H)	Carries Greycode from the front panel knob to the I/O Processor's Front Panel Knob Circuitry.
KB(H)	Carries Greycode from the front panel knob to the I/O Processor's Front Panel Knob Circuitry.
KBSEL(L)	Keyboard select signal sent from I/O Processor to clock keyboard status through the Keyboard's readback buffer, back to the I/O Processor.
LCP(L)	The Display Board's latch clock pulse used when the I/O Processor reads from the Display RAM latch through the I/OP-Display RAM Interface.
LEVEL DISABLE(H)	The Trigger's sequence signal disabling Trigger when high true.
LOAD(L)	The Display Board's counter load signal used to pre-load the horizontal scrolling address counters.
LOADS(L)	The Display Board's load shift register signal used when converting character, cursor, and highlight parallel data to serial data.
LOE(L)	The Display Board's latch output enable signal used when the I/O Processor reads from the Display RAM latch through the I/OP-Display RAM Interface.
LOW SELECT(L)	The Display Board's circuitry select line used when the I/O Processor writes to the horizontal scrolling registers.
LSEL(L)	LED select signal sent from the I/O Processor to clock front panel LED information through the Keyboard's Menu LED Key latch.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
MA0(H)-MA5(H)	The 18-Channel's miscellaneous address lines; used during read-back of acquisition RAMs, programming of front end hybrids, etc.
MAP(L)	The 9-Channel's memory address pointer enable signal derived from Control Processor control signals; used to gate the MAP value through the Status Monitor onto the BCD data bus.
MAP READ(H)	The 9-Channel's memory address pointer read signal derived from Control Processor control signals; used to strobe data from MAP circuitry.
MEAS(L)	Measure signal sent from the I/O Processor to produce a sequential count for scanning the LED/PT matrix.
MEM WRITE(L)	The 9-Channel's control signal that causes storage of data into acquisition storage RAMs.
MF1(L), MF2(L)	Memory full detect signals from the trigger circuitry located on the Control Processor to the Trigger Board; the memory filled value is the number of cycles post-trigger.
M RESET(H)	The 18-Channel's master reset signal to the acquisition memory.
NEW STEP (L)(H)	The Trigger's sequence control signal used to load new sequence values during level changes.
NO CLK(H)	The 9-Channel's flag signal set prior to the occurrence of any acquisition clock; used to hold off the global word recognizer.
NO QUAL(H)	The Trigger's control signal that disables storage qualification at 10 ns on T1.
NOT NO CLOCK(L)	The 9-Channel's flag signal activated when the sample clock occurs and read back by the Control Processor.
N STEP CLK(H)	The Trigger's new step clock signal; goes high when the sequence is being changed.
OE(L)	Output enable signal from the Control Processor to the currently installed RAM pack; used by the processor when reading information from the RAM pack.
OFF(L)	The data off signal derived from Control Processor control lines; used when turning off the data inputs to the Front End Hybrids during initialization.
P0(H), P1(H)	The 18-Channel's acquisition-board-depth control bits used to determine memory chain depth.
PACK(L)	The Control Processor Board's ROM/RAM Data Buffer enable signal.
PINT(H)	Processor interrupt from the Control Processor to the I/O Processor; used to request an interrupt for inter-processor communication.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
PREFILLED 1(L), 2(L)	The Trigger's prefilled signals from Trigger Position Indicators 1 and 2; indicate prefilled storage is complete.
PROBE CLK(H)	The 9-Channel's probe clock used when reading pod I.D.
PROBE ID DATA(H)	The 9-Channel's probe identification information read back from the acquisition probe; carries unique identification code when the probe's POD ID button is pushed.
PROBE R(L)/W(H)	The acquisition board probe identification bit derived from the Control Processor; set during probe I.D. read operation.
PSEL(L)	Processor select signal from the Control Proccessor to the I/O Processor; used during inter-processor communication.
PSET0(H), PSET1(H)	The 9-Channel's acquisition-board-depth control bits used to determine memory chain depth.
Q1(L), Q2F(L), Q2L(L)	The acquisition/trigger system timebase qualifier signals.
QUAL CLK 1(H), 2(H)	The Trigger's qualified timebase 1 and 2 signals used for trigger control.
RAM(L)	Generated by the Control Processor's Select Decode circuitry when accessing Control Processor RAMs; enables the Dynamic RAM controller and, used in conjunction with the SACK(L) signal to control the READY line to the 8088 CPU.
RAM LOW(L)	The Trigger's signal used to select between high and low bytes in function control RAMs (also see TF RAM(L) and ITER RAM (L) descriptions).
RB TRIG(L)	The Trigger's signal to the processor that the 1240 is triggered.
RDA(H), RDB(H)	The 18-Channel's A- and B-side signals used to enable the memory address pointer clocks.
REVC(L)	The Display Board's character attribute signal specifying dark characters on a light background.
RAM LOW(L)	The Trigger's signal used to select between the function control RAMs.
RAS(L)	The Control Processor Board's row address strobe signal used to latch row data into the Display RAMs.
RDA(H), RDB(H)	The 18-Channel's A- and B-side enables for the serial readback clock.
RESEL(L)	The I/O Processor Board's rotary encoder select signal line; used to select the bit value from the front panel knob onto the processor's ND data bus.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
RESET(H)	The Trigger's master reset of trigger commands and controls.
ROM(L)	The Display Board's signal used to enable the character ROM during the character display mode.
RUN(H)	The Trigger's control signal used to enable the acquisition cycle.
SACK(L)	Select acknowledge signal from the Control Processor's Dynamic RAM controller; used in conjunction with the RAM(L) signal to control the READY line to the 8088 CPU.
SE CLK(H)	The Trigger's sequential event clock used to sample sequential word recognizer value.
SEL(L)	The 9-Channel's signal derived from Control Processor control lines; used as a write strobe for loading the aquisition storage RAM select register.
SEL0(H), SEL1(H)	Select 0 and 1 signals from the currently installed ROM or RAM pack to the Control Processor; carries address information used to determine memory space selection.
SEL0(L)-SEL8(L), SELC(L)	The 9-Channel's select signals used to enable individual acquisition storage RAMs.
SE LOAD(L)	The 9-Channel's sequential event load signal derived from Control Processor control lines; used when loading sequential word and glitch values into the Sequential Event RAMs.
SEQ NEW STEP(H)	The Trigger's sequence new step signal; goes high during sequence steps.
SEQ RESET(L)	The Trigger's sequence reset signal; goes low during sequence-generated reset.
SER CLK(H)	The 9-Channel's serial data clock signal derived from Control Processor control lines; used when loading serial data into the Front End Hybrids.
SER STB(H)	The 9-Channel's serial data strobe clock signal derived from Control Processor control lines; used to stobe data into the Front End Hybrids.
SET HOLD(H)	The 9-Channel's signal derived from Control Processor control signals; used to initialize RAM write signal.
SET NO CLK(H)	The 9-Channel's signal derived from Control Processor control lines; used as a strobe to initialize the no-clock register.
S EVT STB(L)(H)	The Trigger's sequential event strobe used to sample the event.
SF CLK(H)	The Trigger's sequence signal used to clock the sequential filter.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
S FILT(L)(H)	The Trigger's signal indicating sequential filter count is satisfied; for action goes (L), for readback goes (H).
SF RAM(L)	The Trigger's control line used to load the sequential RAM.
SGR*(H)	The acquisition board's sequential glitch recognizer signal; when active it indicates the recognition of current sequential glitch. The asterisk denotes a letter that changes when moved from acquisition slot to slot.
SGR POL(H)	The Trigger's sequential glitch recognizer polarity control (for ON/ON NOT selection).
SWR POL(H)	The Trigger's sequential word recognizer polarity control (for ON/ON NOT selection).
S IT(L)	The Trigger's signal indicating the iteration count is satisfied.
SKCLR(H)	The I/O Processor Board's soft key clear signal line; used only during diagnostics to clear the soft key register.
SKENABLE(H)	The I/O Processor's soft key enable signal; used during diagnostics to disable the soft keys.
SKSEL(L)	The I/O Processor Board's soft key select signal line; used to select the conditions of the soft key boxes onto the processor's ND data bus.
SKSET(L)	The I/O Processor Board's soft key set signal line; used only during diagnostics to force an all high or all low input condition to the soft key register.
S LAT STB(L)(H)	The Trigger's sequential latch strobe used to change or latch the sequence level.
SLEV0(H)-SLEV3(H)	The Trigger's stack level 0 - 3 control signals used to force stack levels during initialization; set to F to run.
SLOW CLK(H)	The 9-Channel's flag set low when a sample clock occurs and cleared when the Control Processor reads it back; indicates master sample clocks are infrequent.
SP0(H)-SP3(H)	The sequence pointer signals from the Trigger Board; used when indexing sequential word and glitch values.
SP LATCH(H)	The Trigger's sequence signal used to latch sequence level readback registers.
SR(L)	The Trigger's signal that indicates the sequential word and glitch recognizers are satisfied.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
START(H)/STOP(L)	The 1240 produces a start signal (A10TP385 for I/O Processor and A9TP117 for Control Processor Board) at the beginning of each diagnostic test that may be used as a trigger signal for an oscilloscope or a logic analyzer. The signal test point is raised to a TTL high logic level at the beginning of each test, and released low at the completion of the test.
STORE EN(H)	The Trigger's control signal used to enable storage qualification.
STR 1(H), STR 2(H)	The acquisition master storage signals that cause the storage of previously sampled data into acquisition RAM.
STR 1, STR 2 RB(L)	The Trigger's readback of storage control signals for timebase 1 and 2.
STR GE(L)	The Trigger's global event signal used in global store on event command.
STR QUAL(H)	The Trigger's control signal used to enable storage qualification.
SWR*(L)	The acquisition board's sequential word recognizer signal; when active it indicates the recognition of current sequential word. The asterisk denotes a letter that changes when moved from acquisition slot to slot.
SWR LD(H)	The 18-Channel's sequence word recognizer load signal; used when loading the sequence word recognizer RAMs.
T1(H), T2F(H), T2L(H)	The acquisition/trigger system timebase clocks.
T1*(H), T2F*(H), T2L*(H)	The 9- or 18-Channel card clock signals that contribute to the making of acquisition/trigger system timebase clocks. The asterisk denotes a letter that changes when moved from acquisition slot to slot.
T2F LAST(H)	The Trigger's timebase 2 signal that indicates which phase of the T2 split clock was last in the acquisition cycle.
T2 INIT(H)	The Trigger's timebase 2 signal derived from Control Processor control lines; used to initialize timebase 2 related circuitry.
TB SEL(H)	The Trigger's sequence control signal used to select the current timebase as TB 1 or TB 2; when active indicates TB 1.
TCLR(H)(L)	The Display Board's timing clear signal used to force two blank character positions to the display when entering the Timing Diagram mode.
TDATA(L)	The Display Board's timing data signal carrying serial data from the Timing Diagram ROM.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
TEST(L)	The I/O Processor Board's signal line used to check the ability of the Z80 CPU to write a value out to the board edge connector and correctly read it back. Also, the 9-Channel's strobe signal derived from Control Processor control lines; used for gating probe and board I.D. data through the Status Monitor.
TFALLING(L)	The acquisition board T clock falling edge indicator; active when the probe C/Q line goes from a logic 1 to logic 0.
TF RAM(L)	The Trigger's load signal for control RAMs containing sequence commands for true and false conditions.
THRESH(L)	The 9-Channel's threshold write signal derived from Control Processor control lines; used when setting the 9-Channel's threshold setting.
THRESH(H)	The 18-Channel's threshold write signal derived from Control Processor control lines; used when setting the 18-Channel's threshold setting.
TIMEBASE(L)	The 18-Channel's timebase selection programming strobe.
TIMING(H)	The Display Board's timing diagram data signal carrying serial data to the Timing Diagram ROM. Also the 9-Channel's signal derived from Control Processor control lines; used as a write strobe for loading timing control values.
TMODE(L)	The Display Board's timing mode signal used to indicate the display is currently generating timing diagrams.
TP1(L), TP2(L)	Trigger Position signals from the trigger circuitry located on the Control Processor to the Trigger Board; indicates zero detection (where zero is the trigger location).
TPI1(H), TPI2(H)	Trigger position indicator 1 and 2 ripple clock signals from the Trigger Board to the Control Processor Board; used to clock upper 8 bits.
TPI1, TPI2 RESET(H)	The Trigger's master reset signals for the Trigger Position Indicator counters.
TPG GL(L)	The Trigger's control signal used to specify glitches on the Test Pattern Generator.
TPG T1(H)	The Trigger's control signal used to specify either T1 (true) or 12 MHz (false) as the base clock for the Test Pattern Generator.
TPG T1 CLK(H)	The Trigger's T1 signal for the Test Pattern Generator clock in TPG modes 2 and 3.
TPR0-7(H)	The Trigger's TPI 1 and 2 prescale readback.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
TRAN(H)	Carries multiplexed LED/Phototransistor information from the Keyboard to the I/O Processor's Soft Key circuitry.
TRIG(L)	The Trigger's signal to the Trigger Position Indicators that indicates a trigger has been identified.
TRIG EN(H)	The Trigger's control line used to enable triggering.
TRIG IMM 1(H), 2(H)	The Trigger's trigger immediate control signals to disable data pre-trigger holdoff.
TRIG IN(H)	Trig In signal line carries the buffered, level-shifted trigger signal from the CRT Drive to the Trigger Board.
TRIGGER IN(H)	Trigger In signal line carries an external trigger signal from that rear panel connector in to the CRT Drive's Trig In Level Shift and Buffer circuitry.
TRIG OUT(H)	Trig Out signal line carries a trigger signal from the Trigger Board to the CRT Drive's Trig Out Level Shift and Buffer circuitry; indicates the 1240 attempted to trigger.
TRIGGER OUT(H)	Trigger Out signal line carries a buffered, level-shifted trigger signal from the CRT Drive's Trig Out Level Shift and Buffer circuitry to the rear panel connector.
TRIG RUN(L)(H)	The Trigger's signal indicating the start of a trigger.
TRISING(L)	The acquisition board T clock rising edge indicator; active when the probe C/Q line goes from a logic 0 to logic 1.
TTSQ(H)	The Trigger's control bit set for Two Timebase Storage Qualification.
VTH	The 9-Channel's threshold voltage signal; read back by the Control Processor to determine if threshold is set in the positive or negative range.
VB(L)	The Display Board's vertical blank signal used to reset the raster counter during vertical retrace.
VBIAS(H)	The 9-Channel's line at 3.65V-3.70V;
VD(L)	The Display Board's vertical drive signal that synchronizes circuitry to the CRT Drive Board's vertical sweep.
VDRIVE(L)	Video drive signal from the Display Board to the CRT Drive Board; used to synchronize the display monitor's vertical sweep.
VERT RESET(L)	The Display Board's vertical reset signal used to reset the sync signal generator after raster 240.
VIDEO(H)	Composite video signal from the Display Board to the CRT Drive's Cathode Z-Axis Amplifier.

GLOSSARY (cont.)

SIGNAL NAME	DESCRIPTION
VLATCH(H)	The video latch signal from the Display Board to the I/O Processor; used during diagnostics when the I/O Processor reads back Display RAM data.
WE(L)	Write enable signal from the Control Processor to the currently installed RAM pack; used by the processor when writing information into the RAM pack.
WRITE EN(L)	The 9-Channel's write enable signal derived from Control Processor control lines; allows acquisition cycles to store data.
X1(H)-X7(H)	Carry pulses created by the LEDs (in the LED/PT matrix) to Keyboard.
Y1(H)-Y7(H)	Sent from keyboard to sequentially turn on the front panel phototransistors.
ZERO CROSS(H)	The 18-Channel's signal indicating the zero crossing point for the D/A convertor in the Threshold Voltage Generation circuit. (This signal is used during diagnostics.)